DESIGN OF THE FRONT-END ELECTRONICS BASED ON THE MULTICHANNEL IDEAS ASICS FOR SILICON AND GEM DETECTORS

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IDEAS ASICs are designed for the front-end readout of ionizing radiation detectors and produced by commercial fabless IC supplier – Integrated Detector Electronics AS (Norway). IDEAS ASICs are multichannel (32/ 64/ 128) chips; each chip channel has a pre-amplifier, a shaper and multiplexed analogue readout. It is necessary to configure the internal chip registers (if it has a trigger output), control analogue readout and transmit data from each measuring channel to the DAQ System. These are basic functions of Control Unit based on FPGA. Design of the front-end electronics for silicon and GEM detectors consists of IDEAS IC, ADC and Control Unit. Current FEE BM@N configuration (March 2018) is based on the IDEAS ASICs for Forward Si Detector, GEM detectors and CSC. According to upgrade plans for BM@N, FEE for Si beam tracker, Si beam profilometer, Forward Silicon Tracking Detectors also will be based on the same ASICs. This paper presents the design of the front-end electronics of the BM@N Si beam profilometer prototype: Double-sided Silicon Strip Detector – a coordinate plane with 64x64 measuring channels; IDEAS ASICs – the front-end readout of DSSD; Analog Devices ADC; FPGA Xilinx – Control Unit.

Keywords: Front-end electronics, IDEAS ASICs, Silicon Detectors, GEM Detectors

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1. Introduction

BM@N is an experimental setup in the Nuclotron fixed-target hall with the final goal to perform a research program focused on the production of strange matter in heavy-ion collisions at beam energy range from 2 to 6A GeV [1]. Current Front-end electronics (FEE) BM@N configuration (March 2018) is based on ASICs provided by commercially company IDEAS (Norway) for the following detectors:

- Forward Silicon Detectors;
- GEMs (Gas Electron Multiplier);
- CSC (Cathode Strip Chamber).

2. BM@N detector upgrade

2.1 Forward Silicon Tracking Detectors

Forward Silicon Tracking Detectors consist of 3 coordinate planes: 10, 14, 18 detector modules. Each detector module has 1280 channels and consists of Double-sided Silicon Strip Detector (DSSD) and Readout Cards with 5 VATAGP7.1 IDEAS ASICs for P side of DSSD and 5 – for N side. Each VATAGP7.1 chip has 128 channels. The total number of measuring channels is 53760.

2.2 GEM Tracking System

GEM Tracking System consists of 7 GEM planes. GEM plane has 6400 channels: 50 FEE boards, each of them consists of 4 VA163 IDEAS ASICs. VA163 is a 32-channel chip. The total number of measuring channels is 89600.

2.3 Beam tracker and profile detectors

According to upgrade plans for BM@N, FEE for new detectors also will be based on the IDEAS ASICs:

- Si beam tracker (VATA64HDR16);
- Si beam profilometer (VA32HDR11).

3. The design and development of Si beam profilometer prototype

3.1 Si detector

Detector has double-sided microstrip topology with 32x32 mm^2 active area and 300 μm thickness, based on n-type conductivity 4-inch float-zone Si wafers. Pitch for p+ side is 500 μm, for n+ side 500 μm. Number of strips is 64 for each side, with 90 degree stereo angle between strips.

3.2 Block diagram of the FEE for detectors

Block diagram of the FEE for detectors (Silicon detectors, GEMs, CSC) consists of IDEAS IC, ADC and FPGA [Fig. 1]. First of all, FPGA sends control signals to ASIC to configure it, then signals from detector go to analogue ASIC, then are digitized by ADC and collected and stored in FPGA. Then data go to the DAQ System.

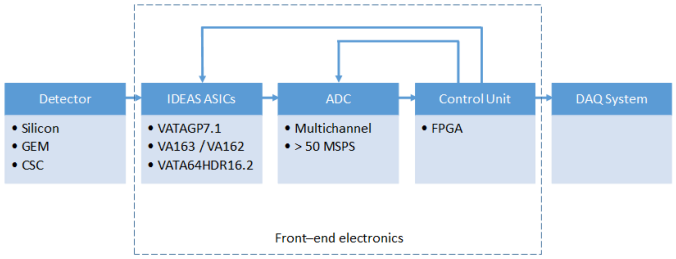

Figure 1. Block diagram of FEE for detectors

3.3 IDEAS ASICs

The table below represents the main features of IDEAS ASICs and its application [Table 1] [2, 3, 4, 5].

Table 1. Application and the main features of IDEAS ASICs

	VATAGP7.1	VATA64HDR16.2	VA32HDR11	VA163	VA162
Number of channels	128	64	32	32	32
Input charges	-30fC ÷ +30fC	-20pC ÷ +55pC	-35pC ÷ +25pC	-750fC ÷ +750fC	-1.5pC ÷ +1.5pC
Shaping time	500ns	50/100/150/300ns	0.9µs	500ns	2 ÷ 2.5µs
Noise	70e^- ENC + 12e^-/pF	1fC	13000e^- ENC	1797e^- ENC at 120pF load	2000e^- ENC at 50pF load
Gain	20µA/fC	2-gain settings	36µA/pC	0.88µA/fC	0.5µA/fC
1 analogue multiplexes output	✓	✓	✓	✓	✓
Time-to-amplitude converter		✓			
Self-trigger	on-chip		with IDEAS TA32cg2		
Application	are used for Forward Silicon Detectors	will be used for Si beam tracker	will be used for Si beam profilometer	are used for GEMs, CSC	were used for GEMs, CSC

All IDEAS ASICs have similar functional description: pre-amplifier, shaper and multiplexed analogue readout. Each pre-amplifier output is connected to a shaper, all shaper outputs can be sampled simultaneously and the pulse amplitude can be multiplexed sequentially to the analogue output buffer, and then read one by one from it. To deliver the pulse amplitude from all channels to output, Control unit based on FPGA has to send a readout diagram.

Description of event readout is shown in Fig. 2. VA162 works by the external trigger. For example, signal from the 3rd strip of the Si detector goes to the VA162 pre-amplifier, then to the fast

shaper of TA32cg2, which forms a trigger signal, and to the VA162 slow shaper to form signal. To sample the measure energy an external *hold* signal should be sent by the Control Unit and applied by VA162 when its slow-shaper reaches the peak (~2us). The sampled value can be accessed through the read-out circuitry in the Back-End. The outputs of all channels are connected to the inputs of a 32 channel multiplexer. The switches in the multiplexer are controlled by a bit-register, and can be used to read out all channels sequentially. Yellow external trigger goes to FPGA to run green readout diagram, at the same time internal address is incremented by green clock and VA162 forms output signal, which represents input analogue signals from 1st to 32nd.

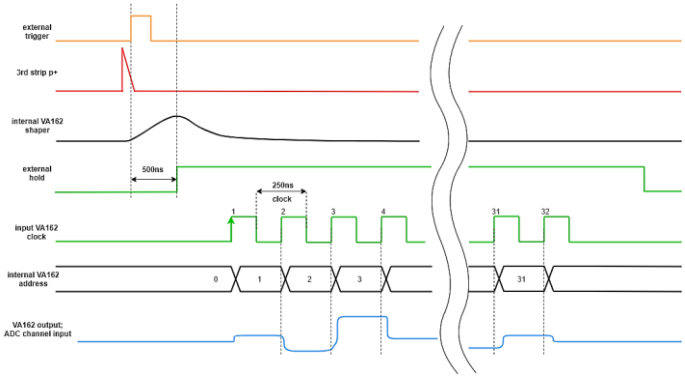

Figure 2. Event readout

3.4 FPGA design

The design of the Control unit based on FPGA is shown in Fig. 3. The main functions are: to configure ASIC registers (from Register block), to send the readout diagram to analogue IC by an external trigger (Sequencer block), to capture and store data from ADC (Capture and Storage blocks), and to send packaged data (Data analyzer block) via USB.

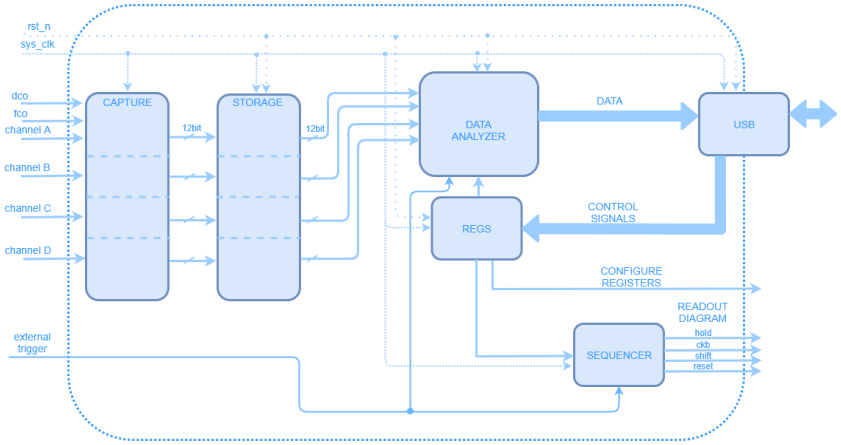

Figure 3. FPGA design

3.5 Design of the Si beam profilometer prototype

Design of the Si beam profilometer prototype [Fig. 4] consists of DSSD (64x64 strips; the size is 35x35 mm^2), analogue IDEAS VA162, trigger chip IDEAS TA32cg2, 12bit Analog Devices ADC9222 and FPGA Virtex4. The sequence of events is as follows:

1. FPGA configures TA32cg2 internal registers: pre-amplifier gain, input polarity, trigger disable for each 64 channels, trigger threshold and test channel;

2. Particle goes to DSSD, the Si detector forms positive signal on the P side, and negative on the N side. Both signals go to VA162 preamplifier, then to the TA32cg2 fast shaper. Also signals from preamplifier go to the VA162 slow shaper;
3. TA32cg2 sends self-triggers to FPGA;
4. FPGA sends readout diagram to VA162;
5. Finally signals from the VA162 output multiplexer are digitized by ADC and packaged and transmitted by FPGA.

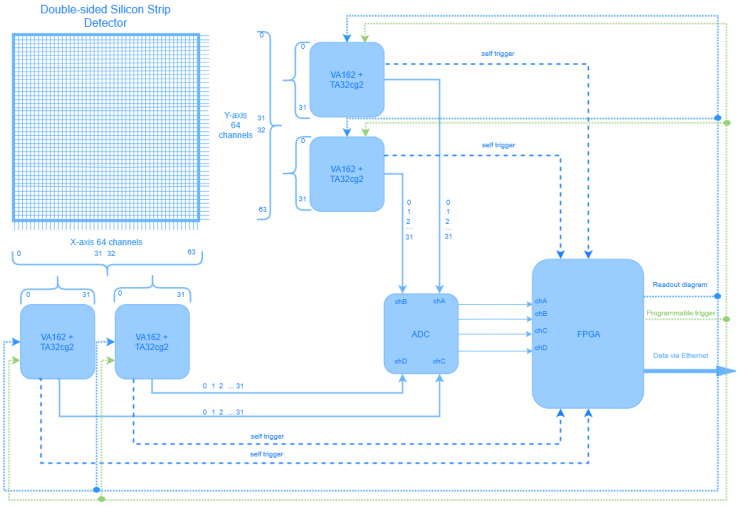

Figure 4. Design of the Si beam profilometer prototype

4. Test results of profilometer prototype with ^{226}Ra

Experimental setup with no vacuum to test profilometer prototype: alpha source, collimator and the Si detector. 1mm of Pb is a collimator, which is placed on the surface of the detector via kapton layer to electrical insulate detector strips. Alpha source is ^{226}Ra. The collimator has 2 holes, which are presented in the profile plot [Fig. 5].

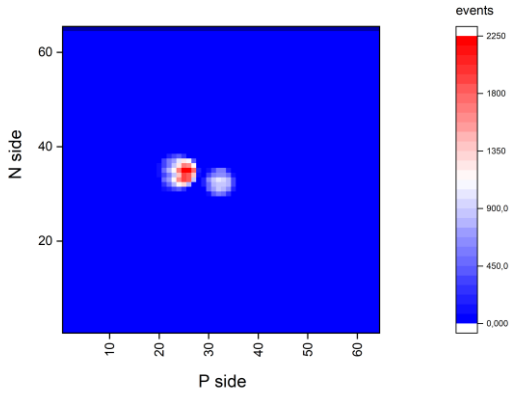

Figure 5. Collimated ^{226}Ra profile

The software was developed to set configurations of VA162 and TA32cg2, display amplitude information and beam profile. ^{226}Ra spectrum with 5 lines (no fitting) and beam profile were obtained from the software [Fig. 6]. Energy resolution of Silicon Strip Detectors depends on the dead layer thickness, which equals 1.5μm (p^+ = 0.4μm + Al = 1μm).

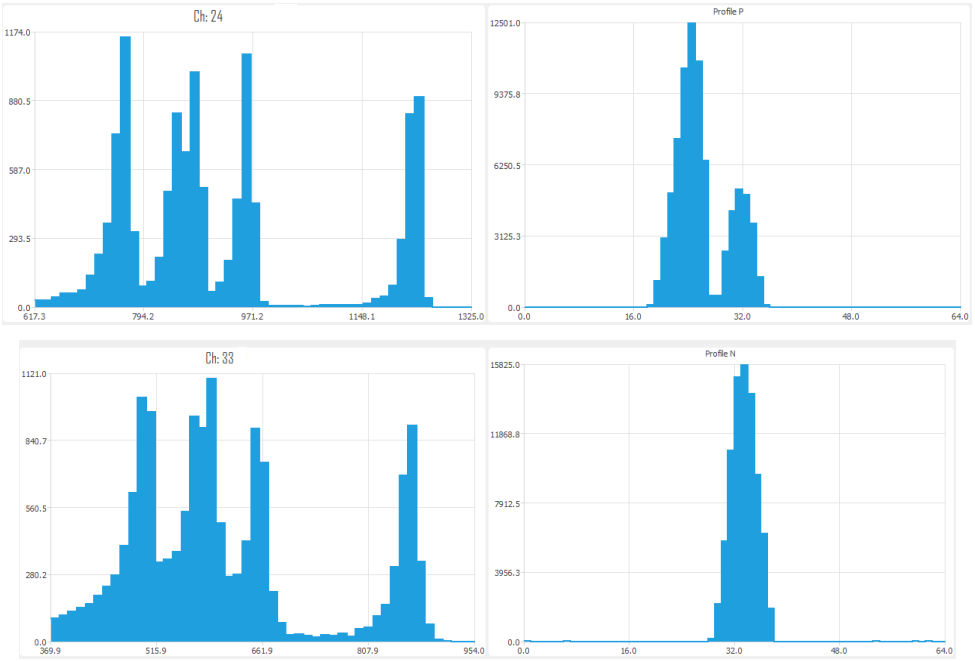

Figure 6. ^{226}Ra spectrum (left) and altha source profile (right) from P side (top) and N side (bottom) of DSSD

As the amplitude from P side of DSSD equals to the amplitude from N side, there is a linear dependence between these two sides of the detector [Fig. 7].

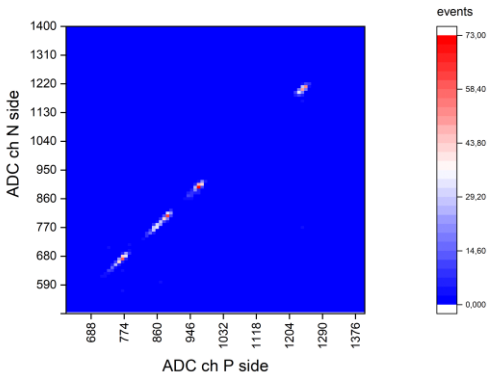

Figure 7. Amplitude correlation

5. Conclusion

IDEAS (Norway) produces multichannel (32, 64, 128), commercially available ICs with a wide input charge range for the front-end readout of ionizing radiation detectors. FEE configuration were based on these chips for Silicon Detector, GEMs, CSC and successfully run for the BM@N

experiment in March 2018. According to the upgrade of the BM@N setup, there was a decision to design and develop the Si profilometer for beam tuning inside the pipe. At the initial stage of work, the Si beam profilometer prototype has been designed and tested with the ^{226}Ra source.

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