PROJECT OF A FAST INTERACTION TRIGGER FOR MPD EXPERIMENT

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The Fast Forward Detector based Level 0 Trigger system architecture is described. The system must provide fast and effective triggering on nucleus – nucleus collisions at the center of the setup with high efficiency for central and semi-central Au + Au collisions. It should identify z- position of the collision with uncertainty better than 5 cm and an event multiplicity in pseudorapidity interval of $2.7 < |\eta| < 4.1$. The system is modular and consists of two arm signal processors and a vertex processor. FPGAs are widely used.

The arm processor crates are located at both sides of MPD magnet yoke to provide minimal cable length and a vertex processor crate is located at the middle of rack line.

Each arm processor receives information from 80 FFD cells and provides preliminary processing of it. The result of pre-processing is sent to the vertex processor. This information includes multiplicity of hits in FFD cells and a time mark signal of the first hit. The arm processor crate also contains a front-end low voltage power supplies.

The vertex processor performs the final trigger processing including estimation of summary FFD hits multiplicity and estimation of Z-coordinate of interaction. The vertex and arm processors contain interface modules with optical links.

Since all this equipment is located in the experimental area and it is exposed to high energy particle irradiation having influence to the FPGA configuration RAM, the processor units containing FPGA are equipped with configuration loading modules. These modules have a library of FPGA configuration files on board and they could provide simultaneous reloading of FPGA RAM to all system FPGAs by a single command...

Keywords: NICA, MPD, Trigger system, FFD

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1.Introduction

Fast triggering of nucleus – nucleus collisions and the precise TOF measurement with picosecond time resolution are important features of all experiments at heavy ion colliders. For these aims a two-arm modular detector with fast Cherenkov or scintillation counters is used.

The Cherenkov Fast Forward Detector (FFD) [1] is an important part of the Multi-Purpose Detector (MPD) setup [2] for study of nucleus – nucleus collisions with beams of the NICA collider [3]. The main aims of the FFD are (i) fast and effective triggering of the collisions in center of the MPD setup and (ii) generation of the start pulse for the TOF detector. A schematic view of the FFD is shown in Fig. 1.

Each FFD sub-detector consists of 20 identical modules with quartz radiators and MCP-PMTs XP85012 from Photonis. Front-end electronics (FEE) board of each module has four independent output channels with signals from MCP-PMT anode pads and one channel with common pulse from second MCP. The inner diameter of the modular array is ~92 mm, the outer diameter is ~360 mm. The FFD sub-detectors are positioned at ±140 cm from the center of the MPD setup.

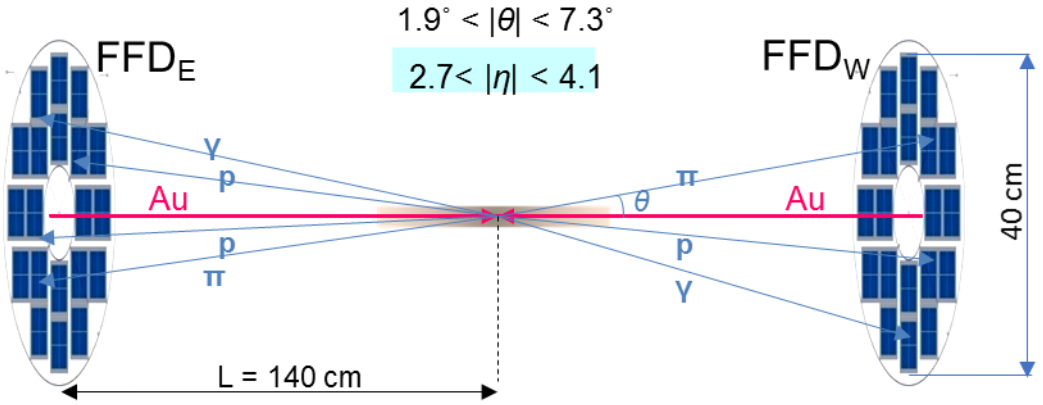

Figure 1. A schematic view of the FFD

The FFD efficiently detects the high-energy photons by their conversion to electrons in a lead plate with thickness of 10 mm located in front of the quartz radiator. Detection of the photons and high-energy pions provides excellent time resolution of the detector with $\sigma < 50$ ps.

2. System hardware

The Fast interaction trigger system consists of three main parts - two Arm Processors (AP) processing data from their subdetectors (module arrays) and a vertex processor (VP). These processors are sitting in a custom VME crates.

The Arm processor receives signals from its subdetector and generate interaction timing signal based on the first arrived module signal and it also calculates multiplicity of hits in subdetector. These data are sent to the vertex processor.

The Vertex processor estimates delay between timing signals from subdetectors and if this difference is less than a predefined value and multiplicity in both subdetectors fulfill requirements then FFD trigger system generates TOF trigger signal.

3.The Arm processor

An AP consists of 4 module pairs providing readout and LV powering of 20 FFD detectors and an Arm Processing Module (APM), see fig. 2.

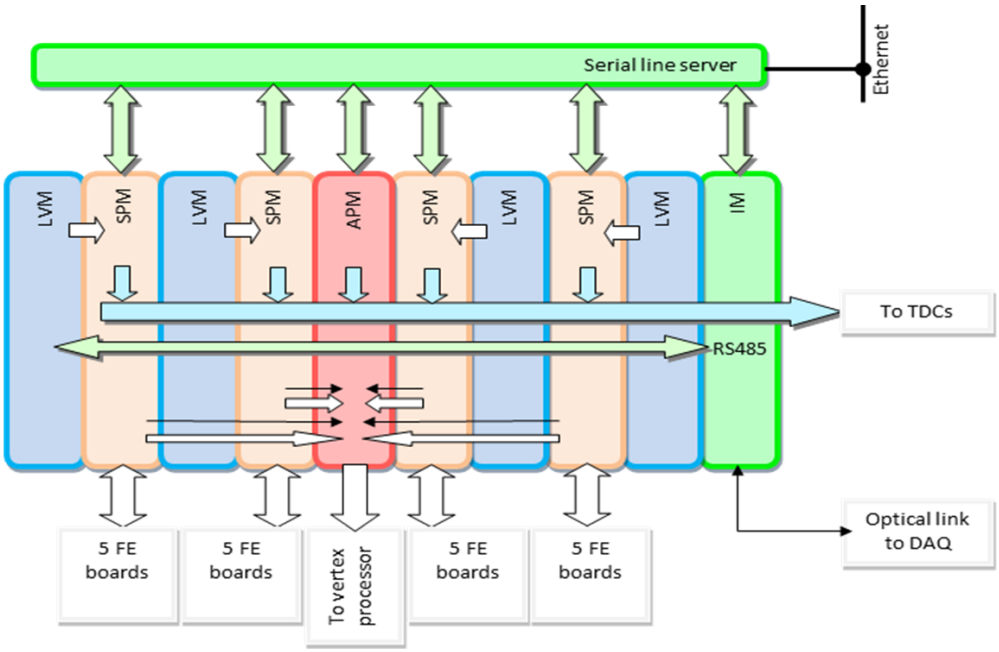

Figure 2. Arm processor

Each pair contains a Low Voltage Module (LVM) and a Signal Processing Module (SPM). The LV power lines go to SPM via a backplane.

SPM receives signals from 5 FE boards and sends LV power to these boards via HDMI cables. Each SPM board contains Cyclone 10 FPGA to process data.

All modules in the AP crate are configured and controlled via RS485 line and their actual state could be read out by the FFD control PC. The data IO speed is 115200 Baud. The interface to the control PC is located in the Interface module (IM) which also has an optical link to DAQ system to receive run control commands and to send actual Arm Processor state to the DAQ data stream.

The LVM provides low voltage power for 5 FE boards. A FE board needs 3 voltages: fixed -7.2 V with current 30 mA and two adjustable +4V...+8V with current 120 mA. The voltage adjustment at positive channels allow to set input signal discrimination level. The voltages are set by 10-bit DAC and channel voltage and current values are read back by 12-bit ADC.

The structure of the individual SPM channel is shown in fig.3.The FE channel signal is split and sent to TDC and to a delay line and then to FPGA logics. The channel contains a pulse width discriminator with approximately 6 ns threshold and 5 ns shaper. The signals from all 5 input channels are ORed and sent to the APM as a timing signal. In addition the SPM logics calculates hit multiplicity and sends this information to the APM too.

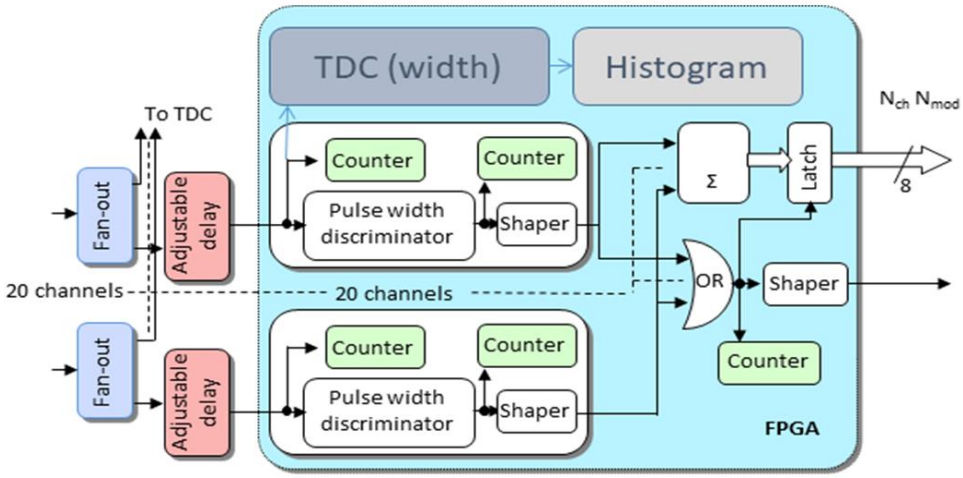

Figure 3. Individual channel block diagram

To monitor the performance of the channel the channel logics contains TDC with approximately 300 ps resolution and range 0-30 ns. The TDC measures input puls width and builds pulse width distribution histogram which could be read-out by the control PC via AP inner serial link.

To align module signal timing according to the geometry of subdetector the SPM contains adjustable presize delay lines with 10 ps step. The delay lines are controlled by a STM32F103 microcontroller.

The APM receives data from SPMs and builds timing pulses and hit multiplicity from whole subdetector and sends it to the Vertex detector.

SPM and APM FPGAs could contain a set of pattern masks to select a required reaction channel triggering.

To simplify FPGA configuration downloading each board equipped with FPGA has a Configuration Loading Module (CLM) which contains a library of FPGA configurations at micro-SD memory card and it is able to load required configuration to FPGA using JTAG protocol. The configuration file name could be set by a command received via individual RS422 line. Typical FPGA configuration loading time is 3 sec. The time required to load FPGA RAM configuration to the CLM memory card library is around 2 minutes. The RS422 data IO speed is 921600 Baud. CLMs are connected to the Ethernet-based serial server device.

The CLM micro-SD memory card has FAT32 file system.

To get a possibility to check SPM and APM signal timing these modules have built-in multiplexers providing signal extraction from FPGA logics key points. These signals are read-out by CAEN digitizers in the real time mode or could be sent to an oscilloscope.

4.The Vertex processor

The Vertex processor estimates a Z-coordinate of an event analyzing time difference between timing pulses arrived from both subdetectors. If time difference is less than a predefined value then the event is marked as "good" and hit multiplicity and pattern are taken into account. If all requirements are fulfilled then the VP generates Trigger Level 0 signal and a TOF trigger signal. The simplified block diagram of Z-coordinate estimation is shown in fig. 4. Alignment delay lines ADL allow to adjust AP signal arrival time and Timing Delay line TDL defines Z-coordinate range.

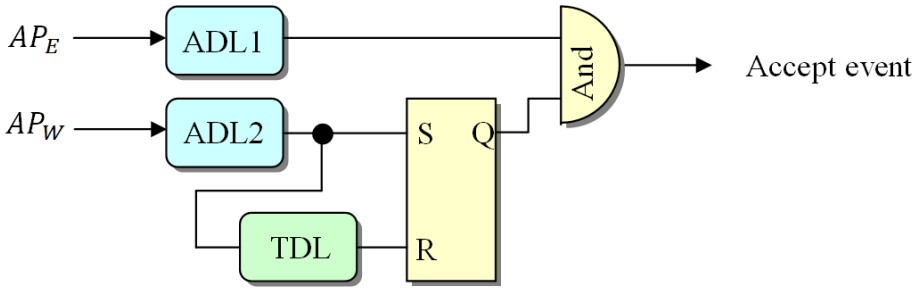

Figure 4. Simplified diagram of interaction Z-coordinate estimation

The VP elements are controlled by STM32F103 microcontroller. The data IO is performed via crate internal RS485 data bus. This data line allows to set delay lines, to read accumulated TDC counts and histograms in the key points of trigger logics.

The VP FPGA is also equipped with CLM.

4.The FFD Detector Control System

The FFD DCS has a client/server architecture. Servers handle the hardware and publish the FFD actual state to all connected clients. Servers also receive commands from local clients running at the FFD control PC and from the MPD Central DCS.

The FFD hardware controlled by FFD DCS includes following components

- HV power supply (Wiener) - 40 channels
- FE LV power supplies (40 units in 2 custom VME crates) – 120 channels
- 2 Arm processors in 2 custom VME crates – 10 FPGAs
- Vertex processor (custom VME crate) – 1 FPGA

- FPGA configuration RAM loading system – 11 modules (CLMs)
- Laser calibration system
- FFD modules temperature monitoring and cooling system (dry nitrogen gas flow)

The FFD configuration has a tree-like structure and consists of set of configurations for subsystems. All configurations are stored in the FFD Configuration DB.

Since the PMTs used in FFD are quite expensive then the full control on HV power supply is permitted only to the FFD stuff. The actual PMT voltages and currents are published but any modification of HV values is possible only via loading of predefined HV configuration. The configuration could be created or modified by FFS experts.

Due to this approach the FFD DCS could accept very limited set of commands

- STDBY – stop HV and laser
- ON – start HV
- Load_Configuration<Configuration name>– download configuration files to HV, LV, laser and FPGAs
- Depending on the architecture of Level1 trigger system the FFD DCS could have additional commands
    - RUN – to enable level zero trigger generation
    - STOP – to disable level zero trigger generation

The FFD DCS states are

- OFF – any of power supplies is in OFF state
- STDBY – all LV power supplies are ON, HV power supply is OFF
- ON (RDY) – system is ready for operation
- RUNNING - level zero trigger generation is enabled
- NOTRDY – configuration loading in progress (including HV setting)
- ERROR – at least one of subsystems is in error state (for example HV trip) and operator intervention is required.

5.Conclusion

The Fast Forward Detector based Level 0 Trigger system architecture is defined. The main submodules have been prototyped.

At the present moment the AP modules are in production and under debugging. The VP modules development will start soon.

References

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