ELECTRONICS UPGRADE FOR THE CMS CSC MUON SYSTEM AT THE HIGH LUMINOSITY LHC

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Cathode strip chambers (CSCs) are used to detect muons in the endcap region of the CMS detector. The High Luminosity LHC will present particular challenges to the electronics that read out the CSCs: the demands of increased particle flux, longer trigger latency, and increased trigger rate require upgraded electronics boards in the forward region. In particular, both the anode and cathode readout electronics will include full digitization at the beam crossing rate and data pipelining in deep digital FIFOs that provide nearly deadtimeless operation and the capability to accommodate long latency requirements without loss of data. High speed optical links will be used to increase the bandwidth for data between the on-chamber electronics and the back end. Motivated by experience with the present electronics and the expectations for high radiation conditions during operation of the HL-LHC, some novel features are incorporated into this second-generation electronics design to provide increased robustness. Radiation tolerant optical transceivers are used in all on-chamber applications. Due to low reliability of EPROMs after radiation doses in the range of 10 kRad, an alternate capability for programming the FPGAs is included via an asynchronous optical link that can complete the programming with comparable or better speed than the EPROMs. We present the novel features of these electronics along with results from test stands and initial commissioning in CMS with cosmic rays.

Keywords: HL-LHC, electronics, cathode strip chambers

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1. The CMS detector

The Compact Muon Solenoid (CMS) detector [1] is located at one of the four interaction points of the Large Hadron Collider (LHC) accelerator complex at CERN. It is composed of several layers of detectors surrounding the interaction point where the protons collide (fig. 1). The inner part is a silicon tracker, which detects the tracks of charged particles. Next are two calorimeters to measure the energy of the many particles arising from the interaction. A 4 Tesla solenoidal magnet envelops these detectors, bending the trajectory of the charged particles. Finally, a large muon system is interleaved between the iron yoke, which provides a flux return for the magnetic field. The magnet is operated at 3.8 Tesla, resulting in a magnetic field of about 2 Tesla in the muon system.

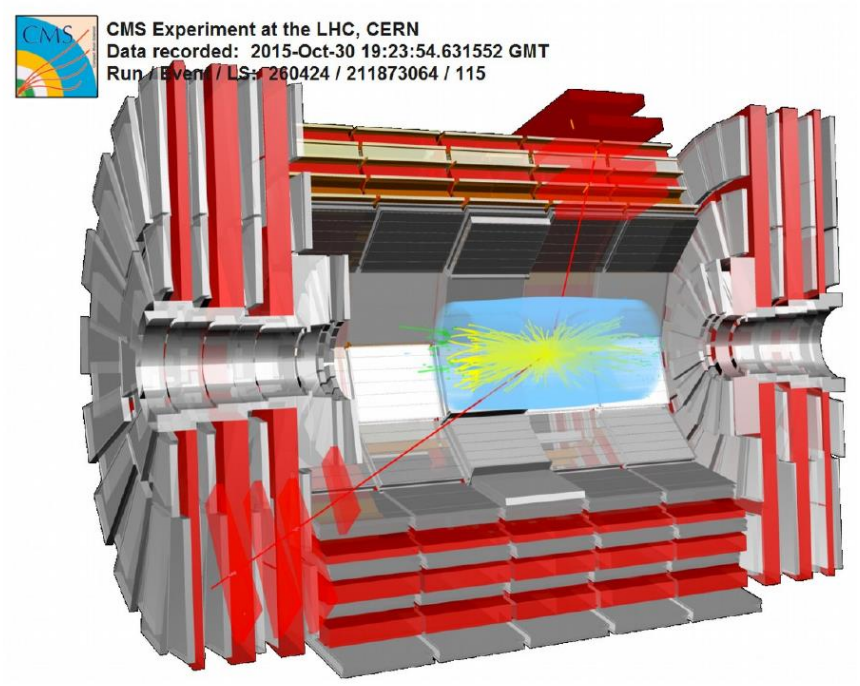

Figure 1. An event display showing two muons traversing the CMS detector. One of the muons is passing through cathode strip chambers in the endcap on the left

The muon system is specifically aimed at detecting muons and consists of drift tubes (DTs) in the barrel part, at low pseudorapidity ($|\eta| < 1.2$) and cathode strip chambers (CSCs) in the endcaps, which cover the high pseudorapidity range ($0.9 < |\eta| < 2.4$). Resistive plate chambers (RPCs) are present in both parts, adding redundancy to the system and providing a good time resolution. These different detector technologies are adapted to their locations by taking into account the higher rate of particles in the endcaps compared to the barrel.

The CSC system consists of 4 stations in each endcap to ensure redundancy on triggering and tracking of muons. Every station is composed of 2 or 3 rings, counting 18 or 36 CSCs each. This amounts to a total of 540 chambers and more than 500,000 channels for triggering and 2D tracking.

2. Cathode strip chambers and their electronics

A CSC is made up of cathode panels segmented into radial strips and anode wires running transversely, forming 6 gas gaps. When a muon passes through the gas, composed of 50% argon, 40% CO_2, and 10% CF_4, it is ionized. The generated electrons and ions drift to the anode wires and toward cathode strips where they are detected as an image charge. The produced signals are then read out and processed by the electronic boards on the chamber (fig. 2). As a result, hits along the trajectory of the muon can be measured in 6 independent layers per chamber.

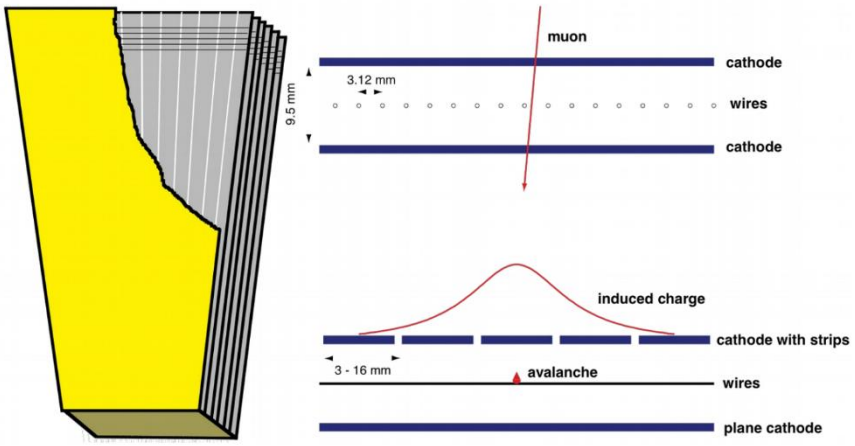

Figure 2. A CSC with 6 layers, with the radial cathode strips and transverse anode wires (left) and the schematic view of a gas gap showing the induced charge by a traversing muon

The strips are read out and processed by the Cathode Front-End Boards (CFEBs), while the wires are read out by the Anode Front-End Boards (AFEBs) and further processed by the Anode Local Charged Track (ALCT) board. The power to all these electronic boards located on the chamber is provided by the Low Voltage Distribution Board (LVDB). These boards communicate with the Trigger Motherboard (TMB) and Data Motherboard (DMB), which are located in the peripheral crates at the periphery of the endcap disks. Finally, the data is sent from the DMB to the service cavern, where the Front-End Driver (FED) crate is situated. The FEDs constitute the interface between the front-end electronics and the global CMS data acquisition system (fig. 3).

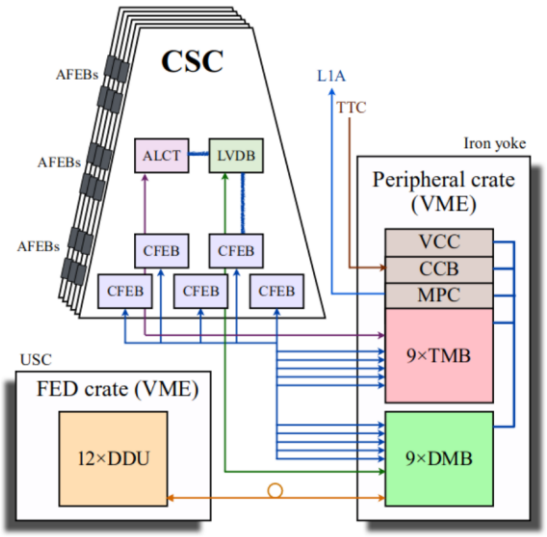

Figure 3. A schematic overview of the CSC electronics showing the boards located on the chamber, away from the chamber in the peripheral crate, and in the CMS service cavern (USC)

3. Electronics upgrade for the HL-LHC

The LHC accelerator will be upgraded by Run 4 (starting in 2026) to increase the instantaneous luminosity of the particle collisions to 7.5 x 10^{34} cm^{-2} s^{-1}, which corresponds to 5 times the nominal LHC value. This upgrade is called the high luminosity LHC (HL-LHC). The accelerator will run at the nominal energy of 14 TeV and CMS will be collecting up to 3000 – 4000 fb^{-1} of data. This upgrade will require CMS to be able to handle a Level-1 (L1) trigger latency of 12.5 μs, due to

the upgraded silicon tracker, which will be included in the trigger [2], and a L1 trigger rate of 750 kHz. The original electronics of the CSCs closest to the beamline are limited by several factors and need to be partially upgraded [3] to be able to cope with these new requirements. The chambers in question are located in the innermost ring of each station and are labeled ME1/1, ME2/1, ME3/1, and ME4/1 (fig. 4).

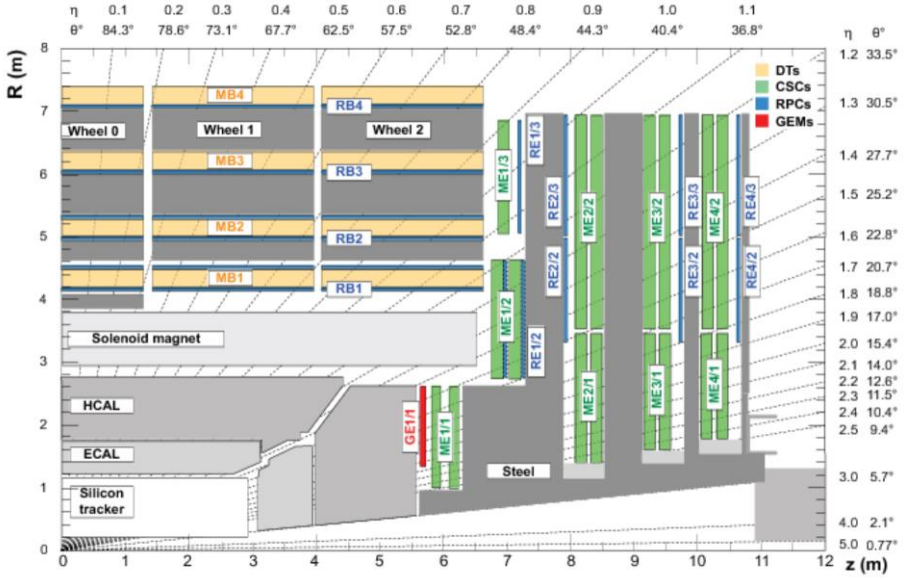

Figure 4. Schematic view of a quarter of the CMS detector showing the location of the different stations and rings of CSCs in green

The current front-end electronics have an insufficient buffer size and cannot handle the longer latency requirements. Additionally, the output bandwidth is too small for the expected L1 trigger rates and occupancies. As a result, a fraction of the data will be lost (fig. 5). In order to overcome this limitation, the CFEBs are being replaced by Digital Cathode Front-End Boards (DCFEBs). The analogue part with the comparator and amplifier and shaper ASICs remains the same as on the CFEB, while the switched capacitor arrays for analog storage of events are replaced. Instead, the DCFEB digitizes all signals through hybrid flash ADCs coupled to a digital pipeline. Additionally, the new boards include remote programming of the FPGA via GBTx to avoid the instances of EPROM corruption that were observed previously.

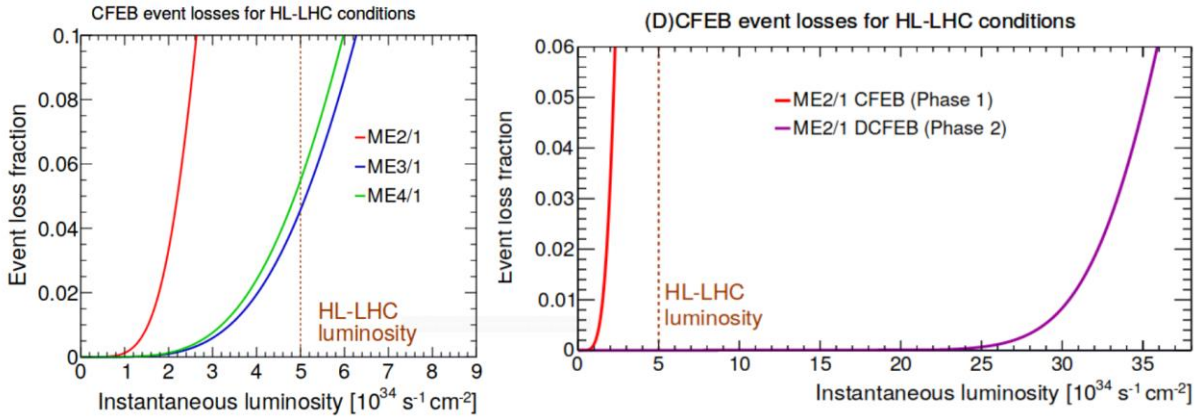

Figure 5. The expected event loss fraction in the ME2/1, ME3/1 and ME4/1 rings with the current CSC electronics as a function of the instantaneous luminosity (left) and a comparison to the expected event loss fraction with the new DCFEB (right)

The mezzanine card of the ALCT board is being upgraded as well, due to the limited output bandwidth and pipeline depth. To provide the appropriate voltages to the new boards on the chambers, the LVDBs are also replaced. To receive the trigger data from the new DCFEBs through the optical fibers, the TMB is being replaced with an Optical Trigger Motherboard (OTMB). This new board also has a more powerful FPGA, providing an increased algorithmic performance. Similarly, the DMBs need to be replaced by Optical Data Motherboards (ODMBs) to receive the data from the DCFEBs through optical fibers and allowing for an increased output bandwidth. Finally, the FED system will also be upgraded to increase the output bandwidth.

An important aspect that is taken into account in the design of the electronics is the radiation hardness. This is relevant for the boards located on the chambers, which receive a significant dose, but also for the TMBs and DMBs located at the periphery of the CMS detector. Therefore, many components such as optical transceivers, regulators, and EPROMs have been tested at several irradiation facilities using neutron, proton, and mixed beams. In addition, the fully assembled boards undergo irradiation tests to confirm that they can withstand the expected total integrated dose at the HL-LHC. Moreover, the susceptibility of the electronics to single-event upsets (SEUs) is studied. SEUs are changes of state caused by one single ionizing particle striking a sensitive node in micro-electronic device. The rate of these events as well as the resulting deadtime are monitored during the irradiation.

The main part of this electronics upgrade is happening during the so-called Long Shutdown 2 (LS2) in 2019-2020. During the next shutdown the upgrade will be finalized by replacing the ODMBs and the FED system.

4. Results from initial commissioning using cosmic rays

After the electronics upgrade, the CSCs need to be tested and recommissioned in order to make sure that the new electronic boards are performing well and the muon detection efficiency remains high. First, extensive testing is performed in the lab immediately after the refurbishment, including data taking with cosmic rays. Following the re-installation of the chambers inside the CMS detector, the electronic boards need to be timed in with respect to each other because of location and cable length. Once the configuration is set properly, the chambers are commissioned by taking data with cosmic rays. Finally, the upgraded system is included in the global data talking, together with other parts of the CMS detector and using the global data acquisition system. The performance is monitored using variables such as hit occupancies and timing (fig. 6).

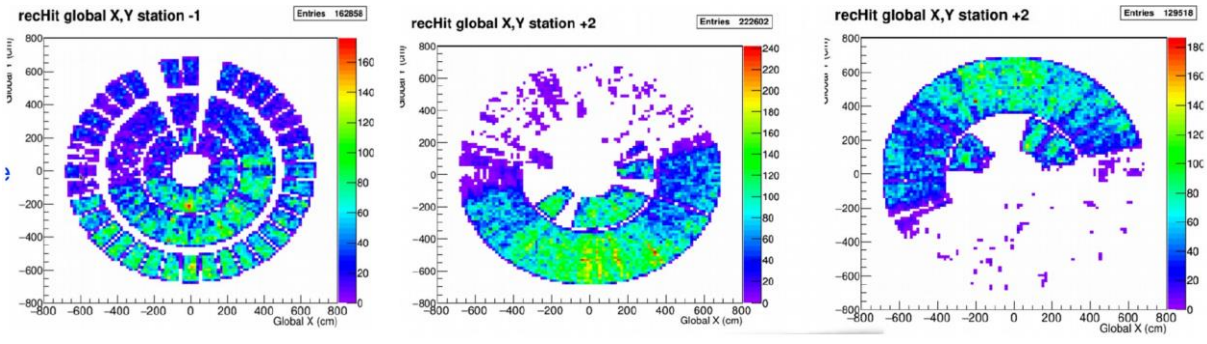

Figure 6. The hit occupancy in station ME-1 during a global run, including the upgraded ME-1/1 chambers (left). The 2 missing wedges were not included in the data talking for this run. The hit occupancy in station ME+2 during a global run, triggering on the bottom (center) and top (right) part of the detector and including the upgraded ME+2/1 chambers. The missing ME+2/1 chambers were not timed in at the time

The results from this initial commissioning show that the refurbished chambers maintain a good performance, as expected. Missing chambers in the occupancy plots were not included in data taking or not timed in yet.

5. Summary

The CMS CSC system is currently undergoing an electronics upgrade in order to be able to cope with the trigger rate and latency requirements and the expected occupancies at the HL-LHC, avoiding data loss in the chambers closest to the beampipe. Half of the chambers have already been refurbished and commissioned and show good performance in runs taken with the global CMS data acquisition system and together with other parts of the CMS detector. The upgrade will be finalized during the next LHC long shutdown, in time for the HL-LHC.

References

[1] CMS Collaboration, "The CMS experiment at the CERN LHC", JINST 3:S08004, 2008

[2] CMS Collaboration, "The Phase-2 Upgrade of the CMS Tracker", CERN-LHCC-2017-009, CMS-TDR-014, 2017, https://cds.cern.ch/record/2272264

[3] CMS Collaboration, "The Phase-2 Upgrade of the CMS Muon Detectors", CERN-LHCC-2017-012, CMS-TDR-016, 2017, https://cds.cern.ch/record/2283189