# Simulation of Logic Elements in Reverse Mode for Building Neural Networks

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### Abstract

The hardware implementation of a feedback neural network, which is based on two ideas: Stephen Grasberg's adaptive resonance theory and Hopfield's auto-associative memory, requires that all elements be connected by direct and feedback connections. This paper presents a simulation of ordinary logic elements, but with reversible properties. The proposed structure allows the signals to move both in the forward and the opposite directions. In practice, this will mean that with the help of control signals, neuron signals can be directed along the same lines of communication in different directions. In this way, all elements of the system will be interconnected and the system will be able to remember and choose the best way to solve the problem.

The authors propose modeling of ordinary logic elements using a special inclusion scheme based on resistive dividers, which allows providing their reversible mode of operation. It is also proposed to use the following logical elements to build neural networks such as the Cosco architecture.

The work simulates the reversible operation of the following logical elements: 1) repeater (buffer); 2) inverter; 3) the logical element NAND; 4) logical element NOR.

### Keywords 1

Logic element, buffer, inverter, NAND, NOR, neural network

## 1. Introduction

The hardware implementation of neural networks is no less important than the development of algorithms and software for the training and operation of artificial intelligence. To build any device or network requires building materials, i.e. a set of similar and simple structural components. In conventional digital technology, structural units are logical elements that can be used to implement any function. In neural networks, such structural units are neurons. Conventional logic elements can also be used to build connections between neurons and some parts of neurons. However, these logical elements must work in reverse mode to ensure the reverse propagation of Verbos [1].

Logical elements with feedback should be used to build fully connected networks. A characteristic feature of neural networks of this type is the presence of connections between all neurons [2, 3]. The most well-known type of fully connected network is Hopfield networks (Fig. 1). In them, each neuron has two-way connections with all other neurons in the network. In the general case, the Hopfield network has a symmetrical ring structure, it is impossible to identify hidden neurons and a single direction of signal propagation. The operation of a fully connected neural network and data exchange is controlled by one main neuron [2].

The main problem that hinders the practical application of most neural networks is the complexity and high complexity of the learning process. The use of reversible logic elements allows you to avoid

adjusting the feedback when learning the neural network. This idea is the basis of Jagger's proposed recurrent neural network ESN (Echo State Network) [4-6], schematically depicted in Figure 2. During its training, only the direct connections of the neurons of the hidden layer with the effectors are modified. The forward and feedback connections between the neurons of the hidden layer do not change. Some ESN models may also have constant feedback between effector outputs and hidden layer neuron inputs.
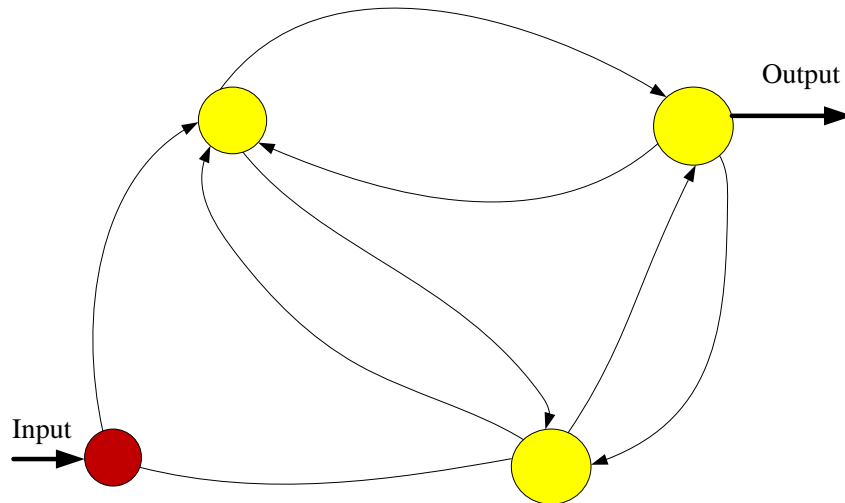


**Figure 1:** Fully connected Hopfield network

In cases where you want to combine two-way communication lines, such as from a programmer or debugger to a microcontroller or between two microcontrollers, you can also use reversible logic elements as a prototype of a fully connected neural network to simplify the circuit [2-4].
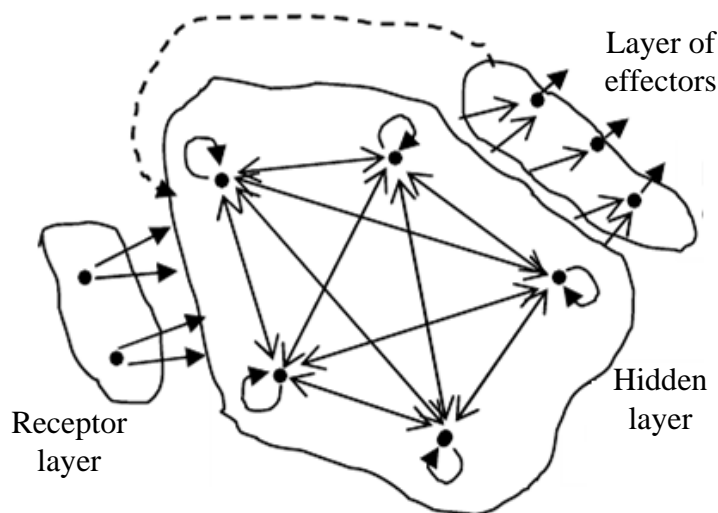


**Figure 2:** Echo State Network

The connections of the hidden layer of the network are established when it is created and are permanent random values. Since only direct connections with effector neurons are modified during training, the responses of effector neurons of the ESN network reflect the linear compositions of the dynamic responses of latent layer neurons [4-6].

To study the circuits of reversible logic elements requires information about the features of their inputs and outputs in normal operation. Today there is a large variety of element base with Z state of outputs, which allows you to easily use them in reverse mode. Elements with three states are widely

used in microprocessor technology to connect the pins of various devices of the microprocessor system to a common bus. However, in some cases, it is interesting and even necessary to use the usual element base in reverse mode. Reversible operation of logic elements allows signals to move along the same line in both directions but at different times. In addition, the signal can be processed by the same logic element, both in the forward and reverse directions. When using the reversible mode of logical elements, it is possible to achieve reversible calculations in the neural network [8-10].

## 2. Inputs and outputs of logic elements

To understand the logic of reversible operation of logic elements, it is necessary to understand the models of inputs and outputs of these elements [11-13].

At the first level of representation of the logical model and even the second level of representation about the inputs of the chips, do not need to know anything at all. The input is considered as an infinitely large resistance, which does not affect the connection of circuit elements. However, the number of inputs connected to one output affects the signal propagation delay.

Even at the third level of representation of the electrical model in most cases, it is not necessary to know about the internal structure of the chip and the circuitry of its inputs. When using a logic zero input signal, a current not exceeding $I_{1L}$ (minimum allowable current) flows from this input, and when a logic unit signal is applied, a current not exceeding $I_{1H}$ (maximum allowable current) flows into this input. In addition, for the correct logic of the chip, it is enough that the voltage level of the input signal of the logic zero was less than $U_{1L}$, and the voltage level of the input signal of the logic unit was greater than $U_{1H}$.

A special case is a situation when any input is not connected to any of the outputs, or the common wire, or the power bus (the so-called hanging input). Sometimes the capabilities of the chip are not fully used, and some inputs do not send signals. However, the chip may not work or work erratically, as its proper inclusion implies the presence of logic levels at all inputs. When such a chip is used in a neural network, all outputs must always be used for signal processing.

The outputs of the chips are fundamentally different from the inputs in that taking into account their features is necessary even at the first and second levels of representation.

There are three types of output stages, which differ significantly, both in their characteristics and in application [11].

1. Standard output or output with two states (denoted by 2C, 2S or, less frequently, TTL, TTL);
2. Output with an open collector (denoted OK, OC);
3. Output with three states or (high-impedance, Z-state) with the possibility of disconnection (denoted by 3C, 3S).

The standard output 2C has only two states: logical zero and logical one, and both of these states are active, i.e. the output currents in both of these states (I0L and I0H) can reach appreciable values. At the first and second levels of representation, such outputs can be considered to consist of two switches that are closed alternately (Fig. 3), and the circuit of the upper switch corresponds to the logic unit at the output and the circuit of the lower – logical zero.
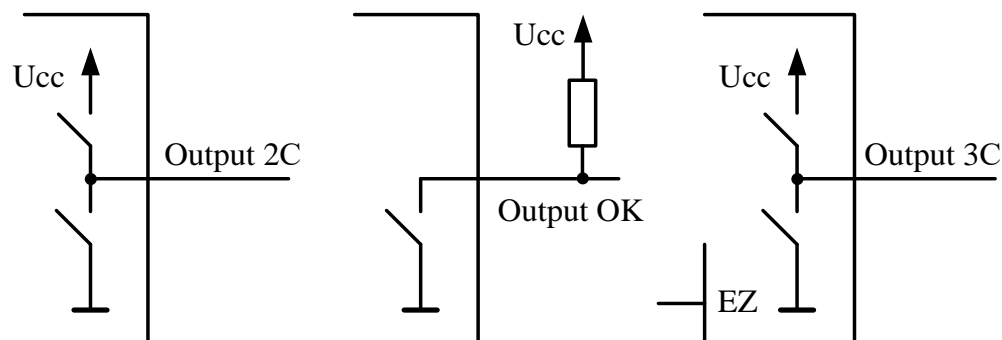


**Figure 3:** Three types of outputs of logic elements

The output with the open collector OK also has two possible states, but only one of them (the state of logical zero) is active, ie provides a large inflow current I0L. The second state is essentially reduced to the fact that the output is completely disconnected from the inputs connected to it. This state can be used as a logic unit, but for this purpose between the output OK and the supply voltage, it is necessary to connect a load resistor R of the order of hundreds of kOhm (in our case 200 kOhm).

The output with three states of the 3C is very similar to the standard output, but to the two states is added a third - passive, in which the output can be considered disconnected from such a scheme. At the first and second levels of representation, such an output can be considered to consist of two switches (Fig. 3), which can be closed alternately, giving a logical zero and a logical unit, but can also open simultaneously. This third state is also called high-impedance or Z-state.

For example, if signals from two outputs need to be applied to the same input in turn (Fig. 4), then outputs 2C are not suitable for this, but outputs OK and 3C are suitable. That is, logic elements with such outputs can be used in reverse mode to build multidirectional neural networks.
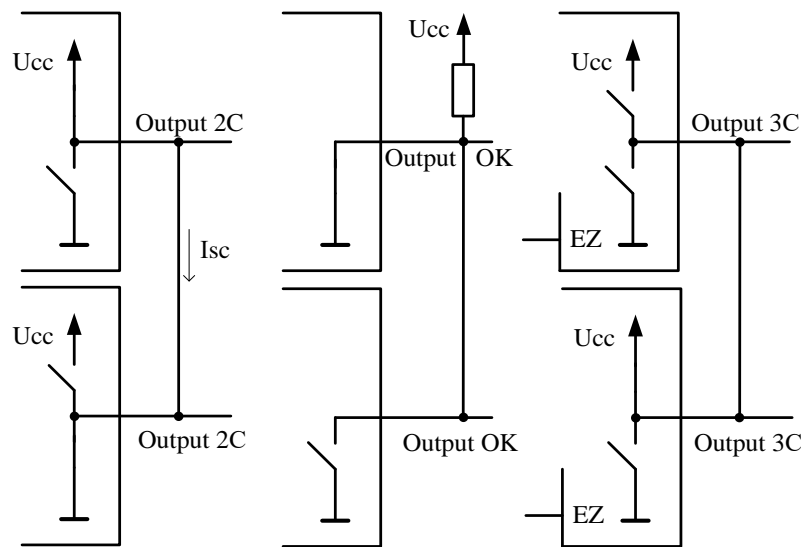


**Figure 4:** Combining the outputs of logic elements

When combining two or more outputs 2C, one output may give a signal of a logical unit, and the other – a signal of logical zero. It is easy to see that in this case, through the upper closed key of the output, issuing one, and through the lower closed key of the output, issuing zero will go unacceptably high short-circuit current Isc. This is an emergency in which the level of the received output logic signal is not precisely defined, it can be perceived by the subsequent input as zero and as one. Conflicting outputs can even fail, disrupting chips and circuits in general. Logic elements with such outputs can be used in reverse mode, but only in special switching circuits that will prevent short circuits.

However, in the case of combining the two outputs of the OK, such a conflict in principle cannot happen. Even if the key of one output is closed and the other is opened, an emergency will not occur, because there will be no unacceptably large current, and the combined output will have a logic zero signal. And when combining two outputs of the Armed Forces, an emergency is possible (if both outputs are simultaneously in the active state), but it can be easily prevented if you organize the circuit so that only one of the combined outputs of the Armed Forces will always be in the active state. [11-13].

Combining the outputs of logic elements in the bus organization of communication between digital elements to form simple neural networks. Most often, the bus organization is used in microcontroller devices; it simplifies the scheme, but is not yet a neural network. This approach allows generalized modeling of neural networks on standard logic elements [2-4, 11].

By bidirectional, lines are understood such lines (wires), the signals of which can propagate in two opposite directions. Unlike unidirectional lines that go from one output to one or more inputs,

multiple outputs and multiple inputs can be connected to a two-way line at the same time (Fig. 5). Bidirectional lines can be organized only based on the outputs of the OK or AP [11-13]. Therefore, almost all buffers have just such outputs. The construction of a neural network implies that all logical elements are interconnected, both at the input and at output. It is the reversible inclusion of logical elements that can provide the hardware of the neural network to provide logical calculations of artificial intelligence [14-17].
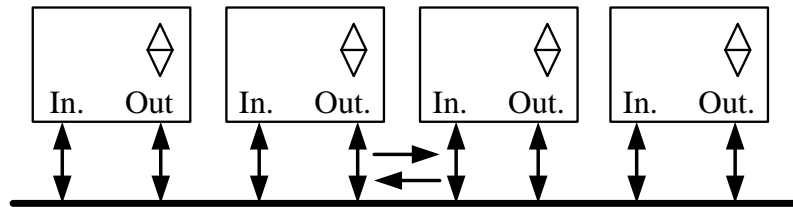


**Figure 5:** Bidirectional line connecting logical elements

A bidirectional line must be multiplexed, and a multiplexed line can be both unidirectional and two-way. In any case, it is joined by several outputs, only one of which at any given time is in the active state. The remaining outputs are currently disabled (switched to passive state). Unlike a two-way line, only one input can be connected to a buffer-based multiplexed line, but necessarily several outputs from the OK or 3C [11].

## 3. Simulation of logic elements in reverse mode in Multisim environment 12

Reversibility in the operation of electronic devices allows equivalent transmission and/or signal processing through these devices in the direction from input to output, and in the opposite direction [14-21], i.e. the inputs and outputs of reversible devices are mutually inverted. The study of the operation of logic elements in reverse mode is to build a switching circuit that allows the logic signal to flow, both in the forward and reverse directions [14-15, 20-21]. To do this, you need to provide a large input resistance at the input of the logic element: more than 50 kOhm and a load resistance of the order of several 100 kOhm. The output resistance to avoid subsidence of the output signal level must correspond to the ratio [20]:

$$Rin \geq 2Rout,$$

where Rin and Rout – input and output pair of reversible logic element.

To ensure minimal amplitude-frequency distortion of the output logic signals, the circuit of the logic elements must be symmetrical, both in input and in output. At such inclusion, logical elements will work equally both indirect inclusion and in return (Figure 6). When a signal source (IN) is connected to terminal *b*, the load to terminal *a* of the logic element will operate in direct connection (input on the left and output on the right). When a signal source (IN) is connected to pin *a*, the load on pin *b* of the logic element will operate in reverse (input on the right and output on the left).
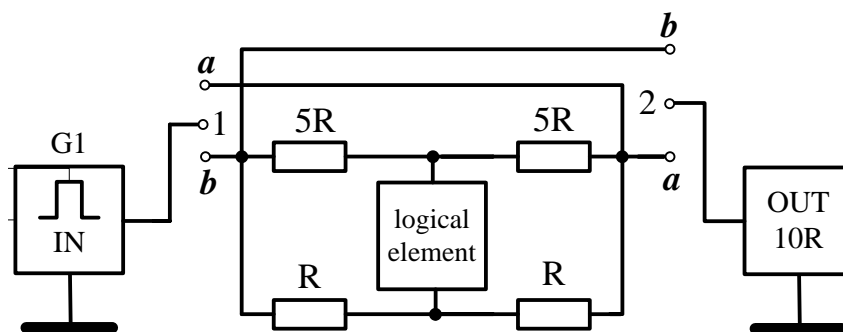


**Figure 6:** Scheme of inclusion of a logical element

If you provide the connection of several inputs of the logic element, the symmetry will be broken, which will lead to a slight distortion of the output signal. However, this will provide information about the current state of the input signals, which will be shown later in the process of modeling reversible logic elements.

## 3.1. The Buffer simulation in Multisim environment 12

Figure 7 shows a diagram of the study of the buffer 4010VS1 in reverse mode. The circuit consists of: a rectangular signal generator G1 with a frequency of 100 kHz and a voltage of 5V; resistors R1 and R3 to provide high input resistance; resistors R2 and R4 to provide output decoupling (matching output resistances); load resistance R5 (signal receiver); switches SA1 and SA2, which act as controllers, determining the input and output of the reversible logic element, in this case, the buffer.
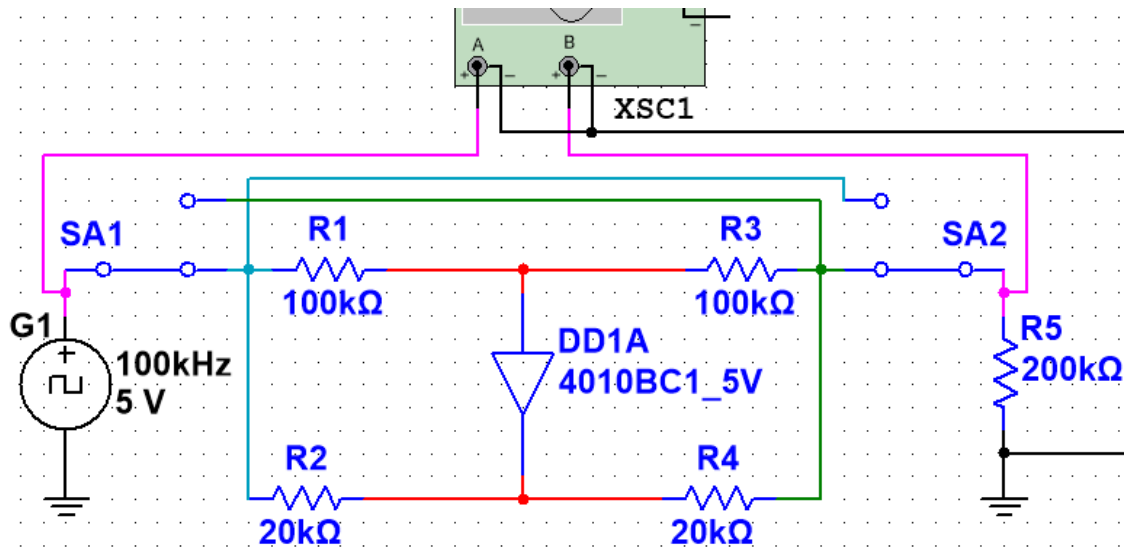


**Figure 7:** Scheme of the study of the buffer direct inclusion

Figure 8 shows the timing diagrams of the buffer indirect inclusion, which show that such a logic element repeats the input signal without significant distortion. The delay of the output signal for the test buffer is 124 ns.

To study the buffer in inverse mode, you need to switch switches SA1, SA2 to the opposite value. In this case, the signal is fed to the right (in the previous scheme it was the input) and removed to the left (in the previous scheme it was the output).
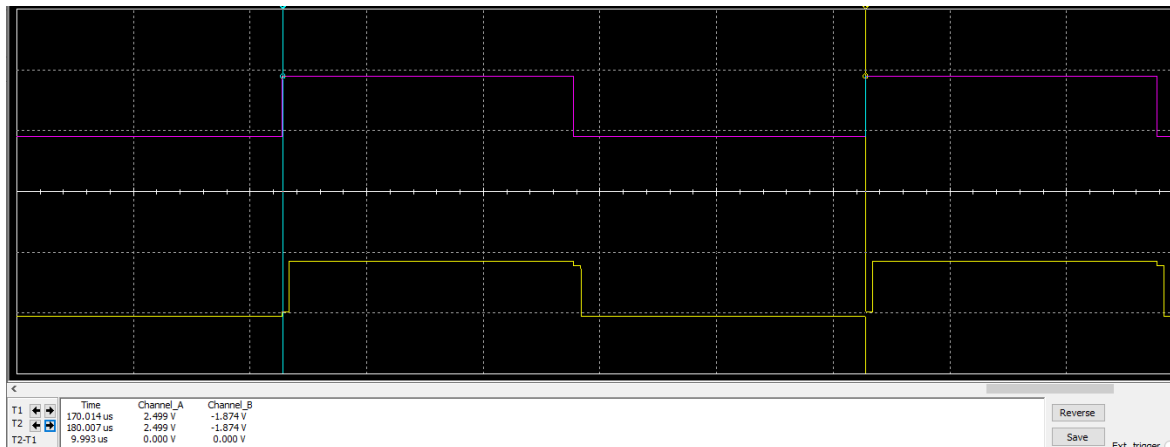


**Figure 8:** The Oscillograms of the buffer in the direct-on mode

The results of the study of the buffer in the inverse mode are shown in Figure 9. The delay of the output signal for the studied buffer is 124 ns.
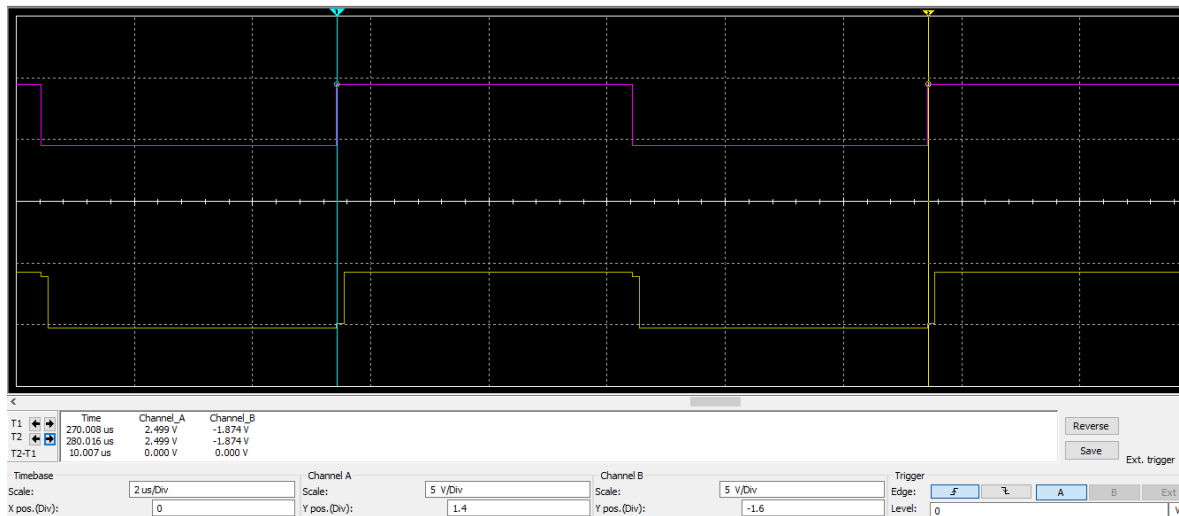


**Figure 9:** The Oscillograms of the buffer in the reverse mode

From Figures 8 and 9 it is seen that the studied circuit of the inverter works the same, both in direct connection and in reverse. It is determined that the output signal delay is 124 ns, and the buffer is limited to a maximum frequency of 100 MHz.

## 3.2. The Inverter simulation in Multisim environment 12

Figure 10 shows the study diagram of the inverter NC7SZU04. The circuit consists of: a generator of rectangular signals G1 with a frequency of 100 kHz and a voltage of 5V; resistors R1 and R3 to provide high input resistance (100 kOhm); resistors R2 and R4 to provide output decoupling (20 kOhm); load resistance R5 (200 kOhm); switches SA1 and SA2, which act as controllers, determining the input and output of the reversing inverter; inverter NC7SZU04.
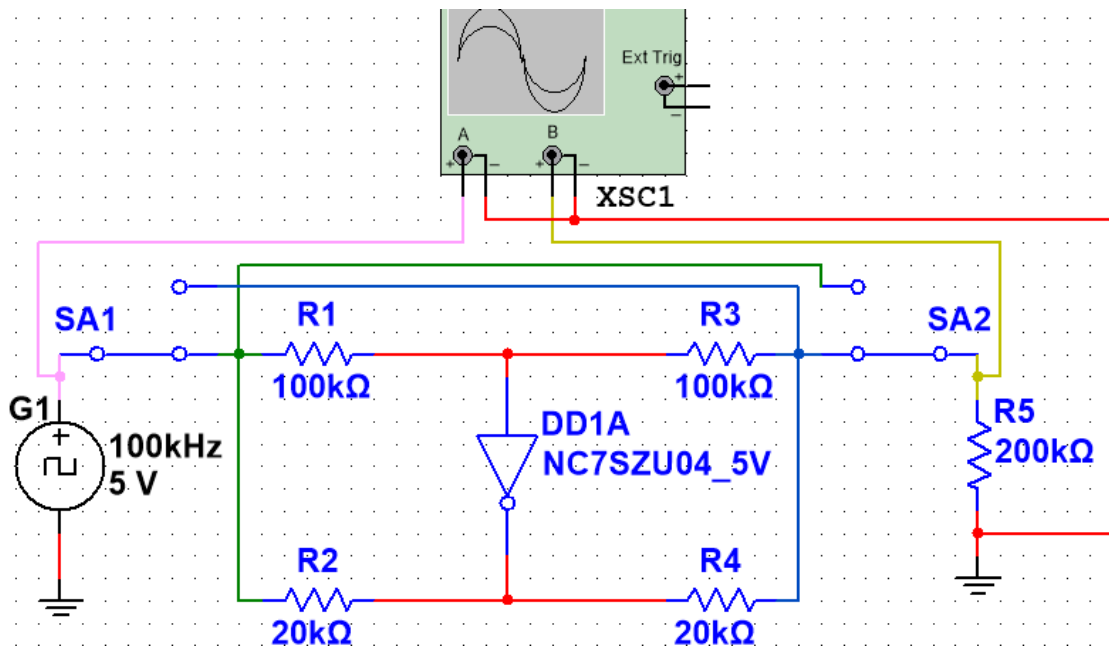


**Figure 10:** The scheme of the study of the inverter direct connection

Figure 11 shows the timing diagrams of the inverter in direct inclusion, which shows that such a logic element inverts the input signal without significant distortion. The delay of the output signal for the investigated inverter is equal to 5ns. Negative voltage output at the beginning of the pulses and positive - at the end of the pulses is 0.3V.
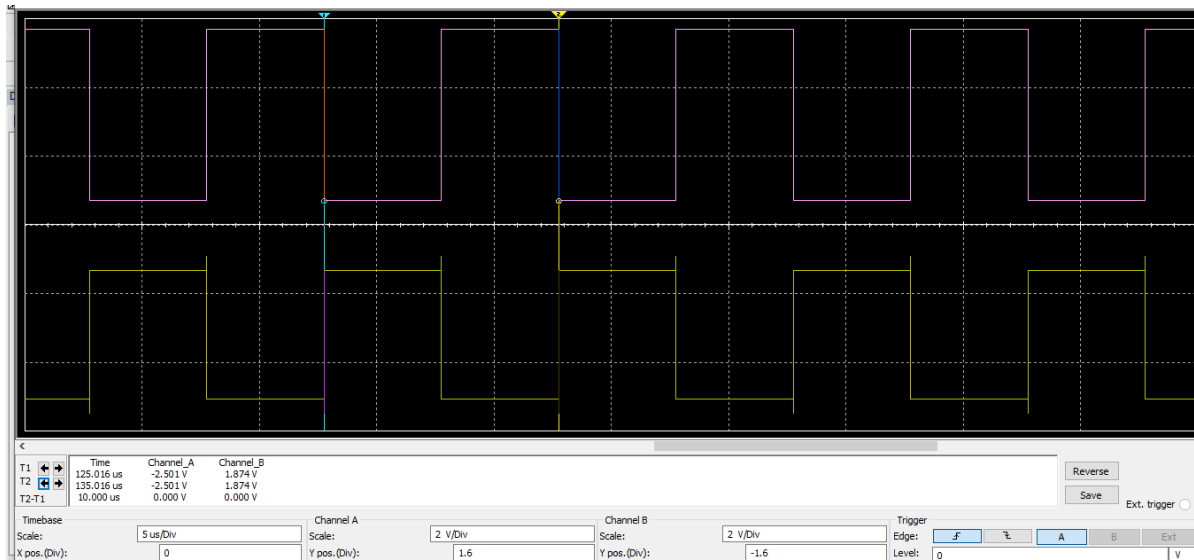


**Figure 11:** The Oscillograms of the inverter in the direct-on mode

Figure 12 shows a study diagram of the inverter NC7SZU04 in reverse inclusion. In this case, the input of the element to the right, where previously there was input, and the output to the left, where previously there was an output. This ensures the reversibility of the investigated logical element.
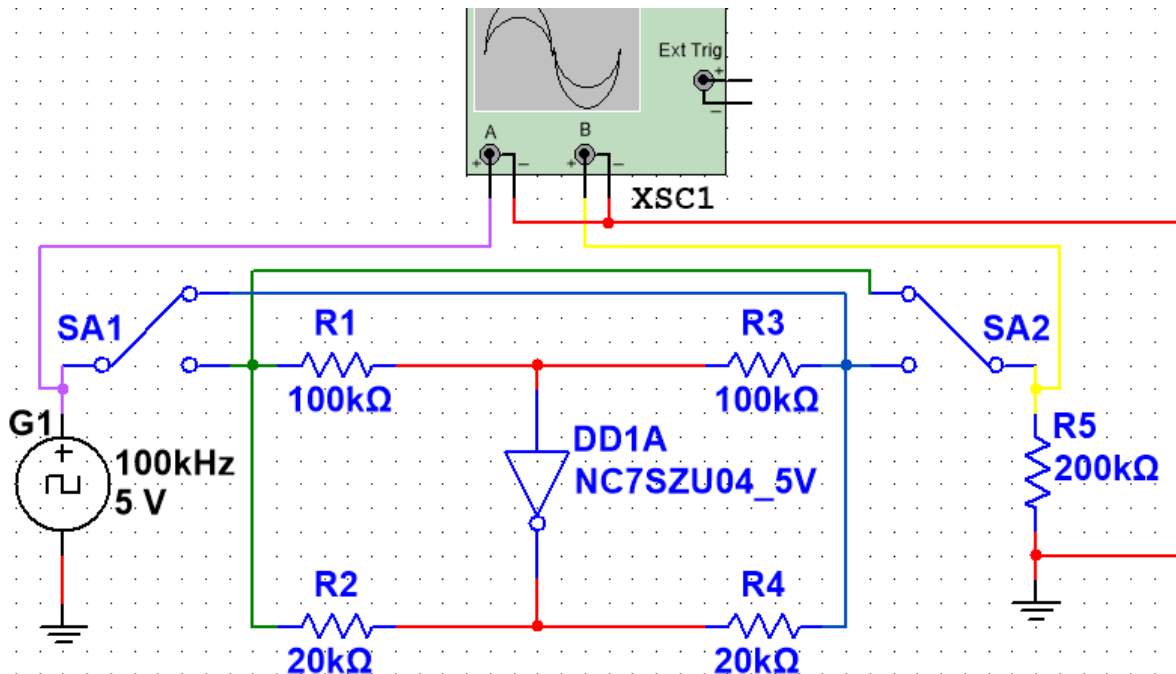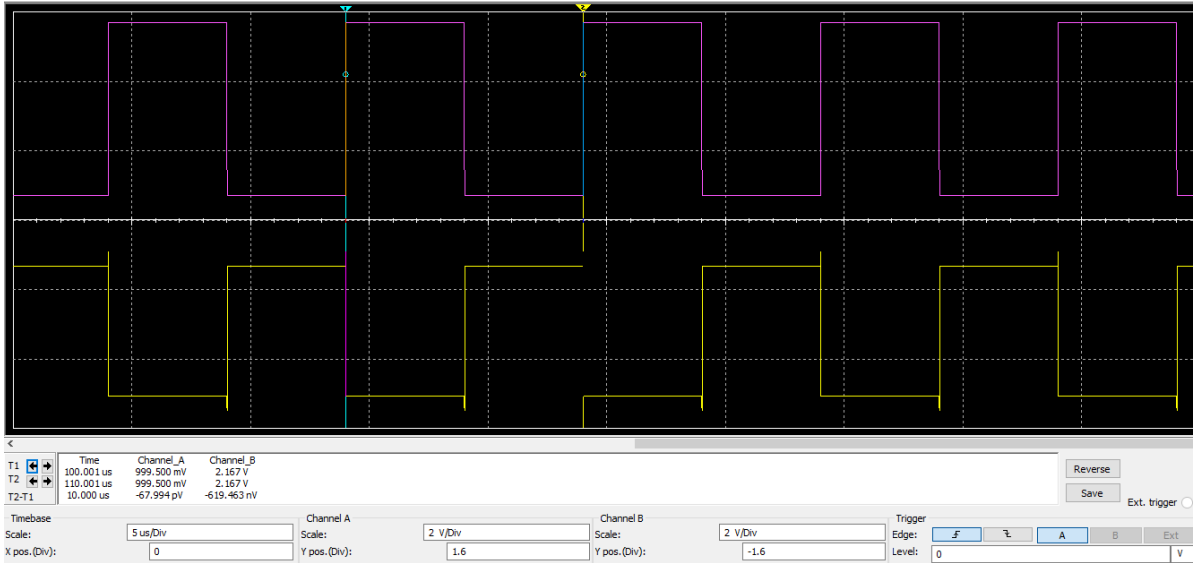


**Figure 12:** The scheme of the study of the inverter in reverse inclusion

Figure 13 shows the timing diagrams of the inverter in reverse switching, which show that such a logic element inverts the input signal with a delay of the output signal of 5.5ns and a negative voltage output at the beginning of the pulses and positive at the end of the pulses 0.32V.
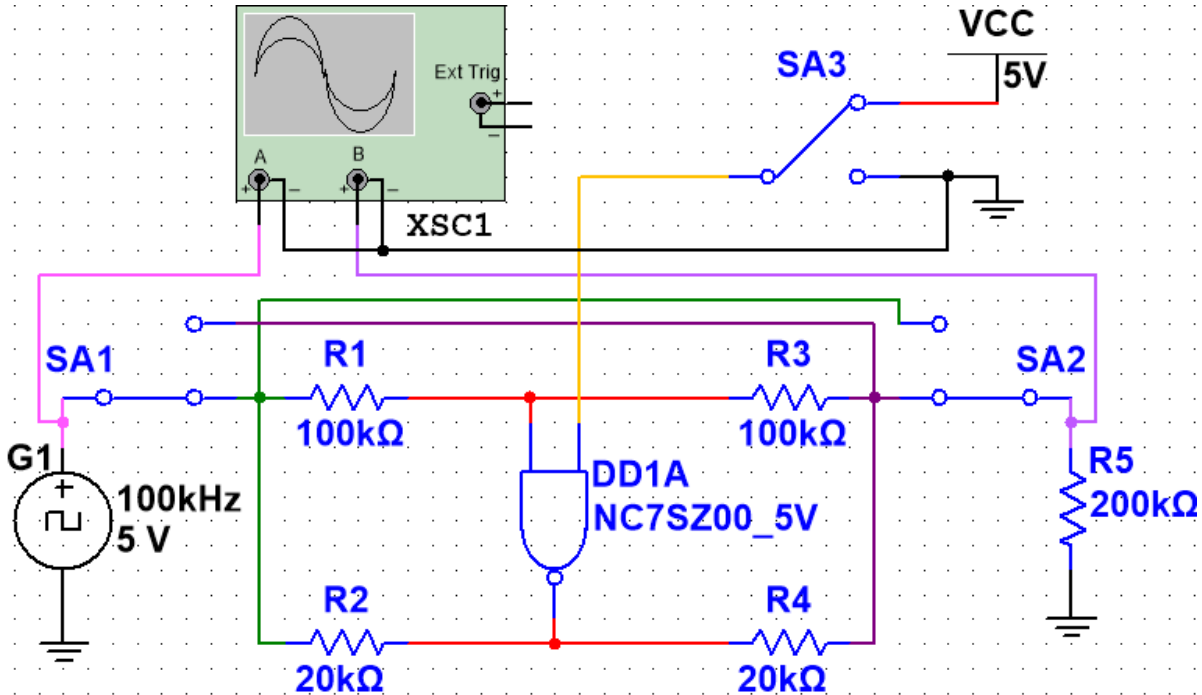
**Figure 13:** The Oscillograms of the inverter in reverse mode

The results of the study of the inverter in reverse mode show that such a logic element works the same in both cases. Although due to the above switching scheme there are some insignificant amplitude-frequency distortions of the output signal (0.3-0.32V), which can be easily eliminated using amplitude limiters.

## 3.3. The Logical element of NAND simulation in Multisim environment 12

Figure 14 shows a diagram of the study of the basic logic element NAND (NC7SZ00) in the mode of direct inclusion. In this inclusion, the logic element NAND (Figure 15) works like a normal inverter with a delay of the output signal of 5.8ns and voltage output of 0.32V.



**Figure 14:** The scheme of research of the logical element of NAND in direct inclusion
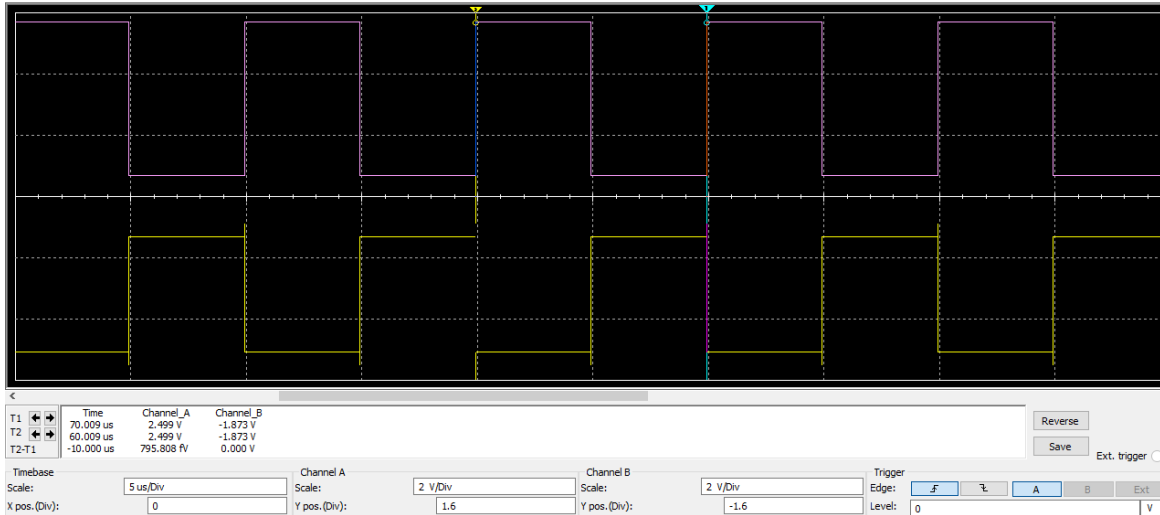
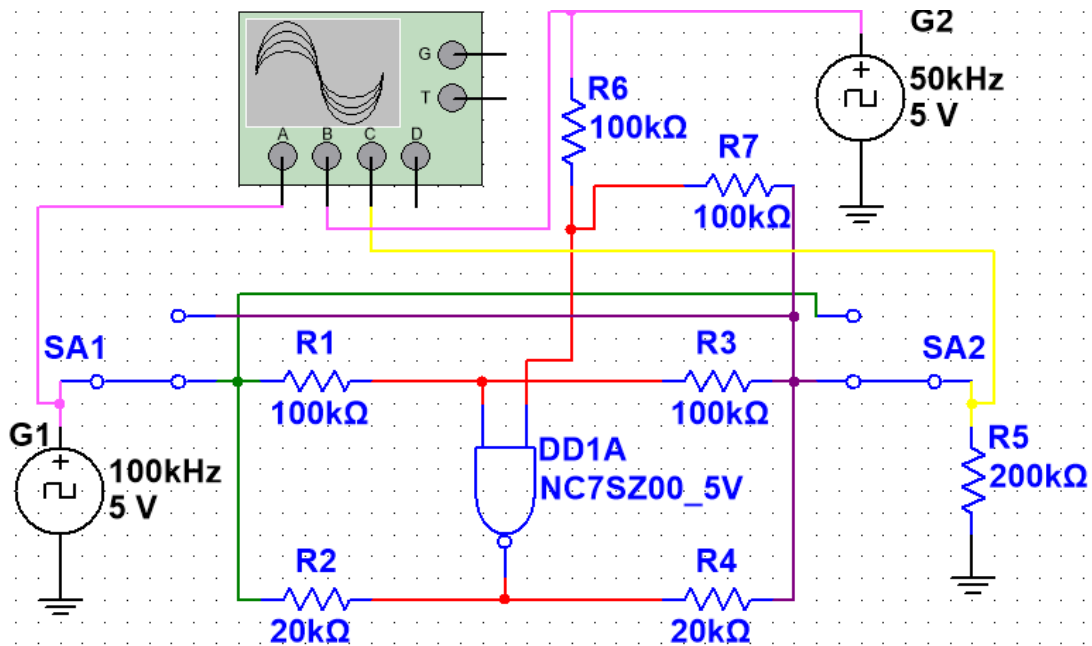**Figure 15:** The Oscillograms of the logical element of NAND in the mode of direct inclusion
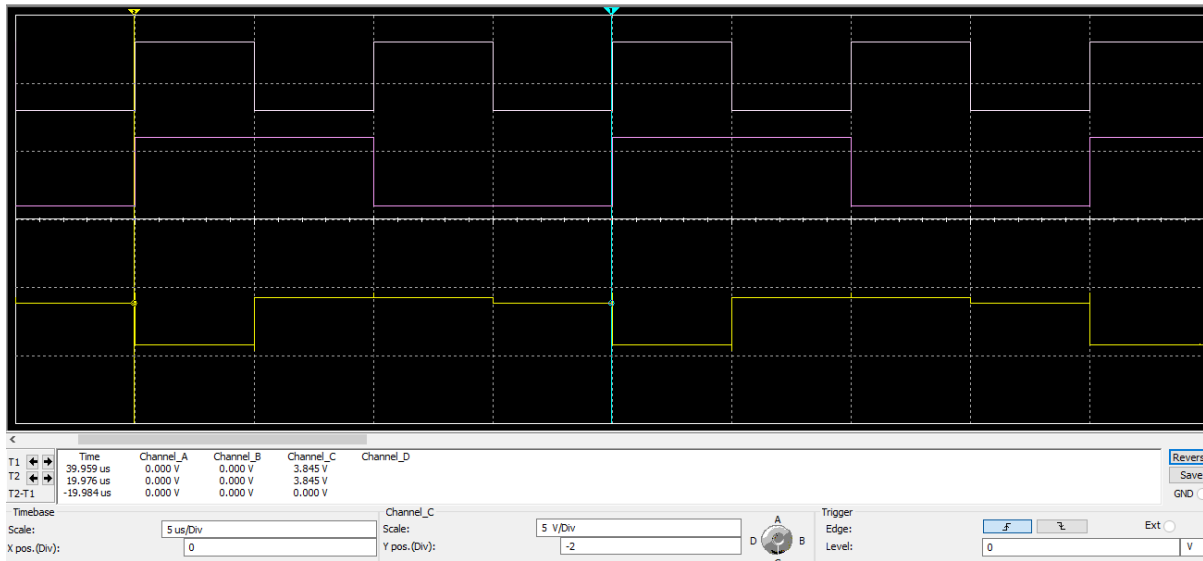
If one of the inputs of the logic element NAND is rigidly set to a value of logical zero, it will not work in normal mode. It will work as a voltage repeater with a significant drop in the level of the output logic signal.

Figure 16 shows a diagram of the study of the logic element NAND NC7SZ00 in direct connection in the case when the inputs are connected to two input signals. The pulse duration of the first signal is 2 times less than the pulse duration of the second signal. That is, the frequency of the first signal is 2 times higher than the frequency of the second signal. This inclusion allows you to explore all possible combinations at the input of the element NAND, both in direct inclusion and in reverse.



**Figure 16:** The Scheme of research of a logical element of NAND direct inclusion, at the connection of two sources of logical signals

Figure 17 shows the timing diagrams of the logic element NAND in direct connection, which shows that the delay of the output signal is 5.8ns, and the amplitude emission is 0.32V. In the pause, the signal differs from the logic zero by 0.32V, now when on both inputs of a logical element logical zero, subsidence of an output signal on 0,32V with a delay of 5.8ns is observed.

| | Time | Channel_A | Channel_B | Channel_C | Channel_D | |
|---|---|---|---|---|---|---|
| T1 | 39.959 us | 0.000 V | 0.000 V | 3.845 V | | Reverse |
| T2 | 19.976 us | 0.000 V | 0.000 V | 3.845 V | | Save |
| T2-T1 | -19.984 us | 0.000 V | 0.000 V | 0.000 V | | GND |

Timebase — Scale: 5 us/Div — X pos.(Div): 0
Channel_C — Scale: 5 V/Div — Y pos.(Div): -2
Trigger — Edge: — Level: 0 — Ext — V

**Figure 17:** Oscillograms of operation of a logical element of NAND direct inclusion at the connection of two sources of a signal with different frequency

Figure 18 shows the timing diagrams of the logic element NAND in the reverse inclusion (in the diagram Figure 16, it is necessary to translate the switches SA1, SA2 in the opposite state). In the pause, the signal differs from the logic zero by 0.32V, now when at both inputs of the logic element logic zero, there is a sag of the output signal by 0.32V with a delay of 5.8ns. At the first input a logical unit, and at the second input a logical zero. In this case, this is due to the transition of the logic signal from the state of logical zero to the state of the logical unit and the violation of the symmetry of the connection of the second input of the logical element NAND.



| | Time | Channel_A | Channel_B | Channel_C | Channel_D | |
|---|---|---|---|---|---|---|
| T1 | 245.007 us | 0.000 V | 5.000 V | 3.499 V | | Reverse |
| T2 | 225.046 us | 0.000 V | 5.000 V | 4.165 V | | Save |
| T2-T1 | -19.961 us | 0.000 V | 0.000 V | 666.444 mV | | GND |

Timebase — Scale: 5 us/Div — X pos.(Div): 0
Channel_C — Scale: 5 V/Div — Y pos.(Div): -2
Trigger — Edge: — Level: 0 — Ext — V
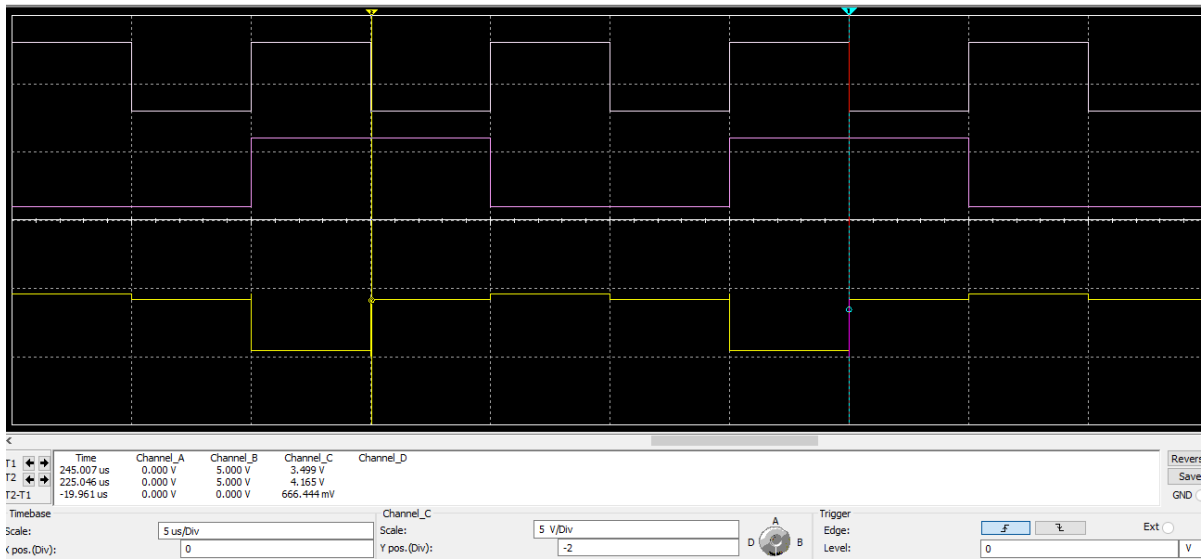
**Figure 18:** Oscillograms of operation of a logical element of NAND in reverse inclusion at the connection of two sources of a signal with different frequency

The results of the study of the basic element NAND show that it can work as an inverter, or as a classical element NAND when applying to its input arbitrary variables in time logic signals. However, it is not able to work in normal mode, when one of the inputs will be rigidly set to logical zero. When this is enabled, it, according to the logic of operation, must always output a logical unit, but works as a buffer, but with a significant sag of the output voltage. The advantage of this switching scheme is

that when analyzing the output signal, namely the analysis of voltage emissions, you can tell exactly what signals were on each of the inputs of the logic element at a particular time, i.e. this element can store information about the input signals in the output logic signals. The circuit of the reversible logic element NAND is limited to a maximum frequency of 200 MHz.

## 3.4. The Logical element of NOR simulation in Multisim environment 12

Figure 19 shows a diagram of the study of the basic logic element NOR (NC7SZ02) in the mode of direct inclusion. In this case, one input is a time-varying logic signal, and the other input is a hard-set logic zero. In this inclusion, the logic element NOR (Figure 20) works like a normal inverter with a delay of the output signal of 6ns and voltage output of 0.28V. If you apply to the second input of a logic element NOR non-logic unit (VCC), then the logic of such an element should always give a logical zero at the output, but it will work as a buffer with a significant sag of the output logic signal. Thus such scheme works equally, both in the mode of direct and in the mode of return inclusion.
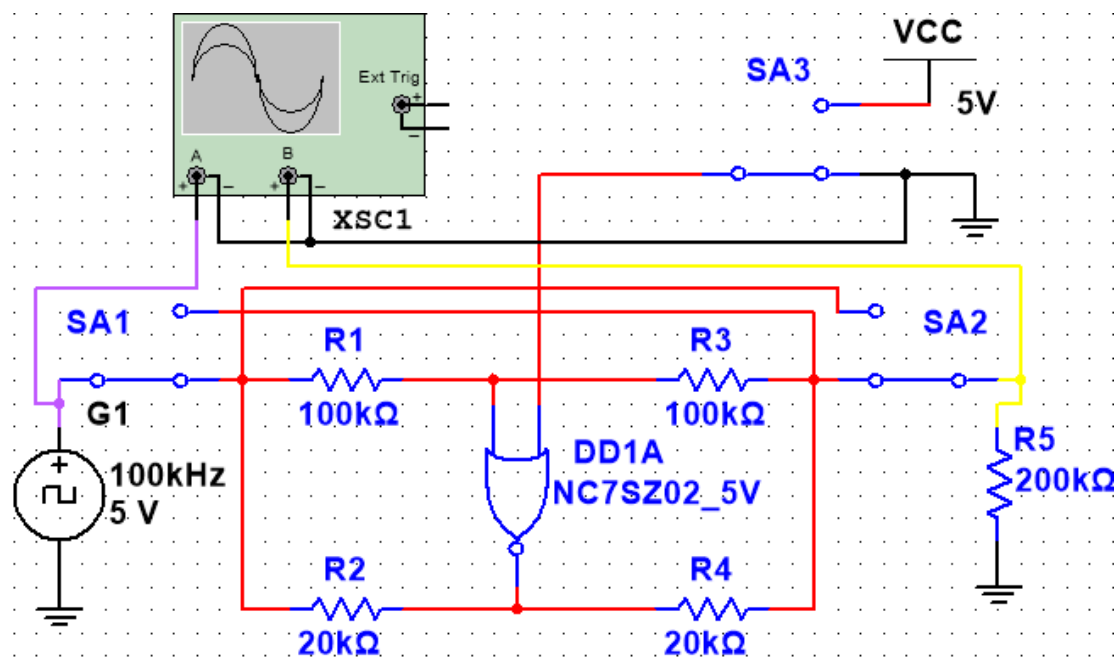


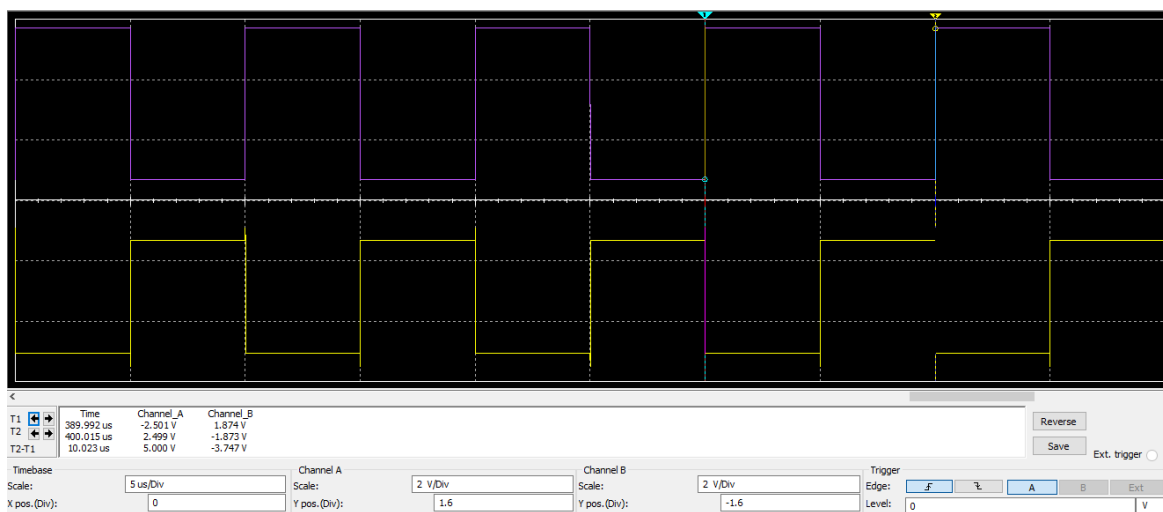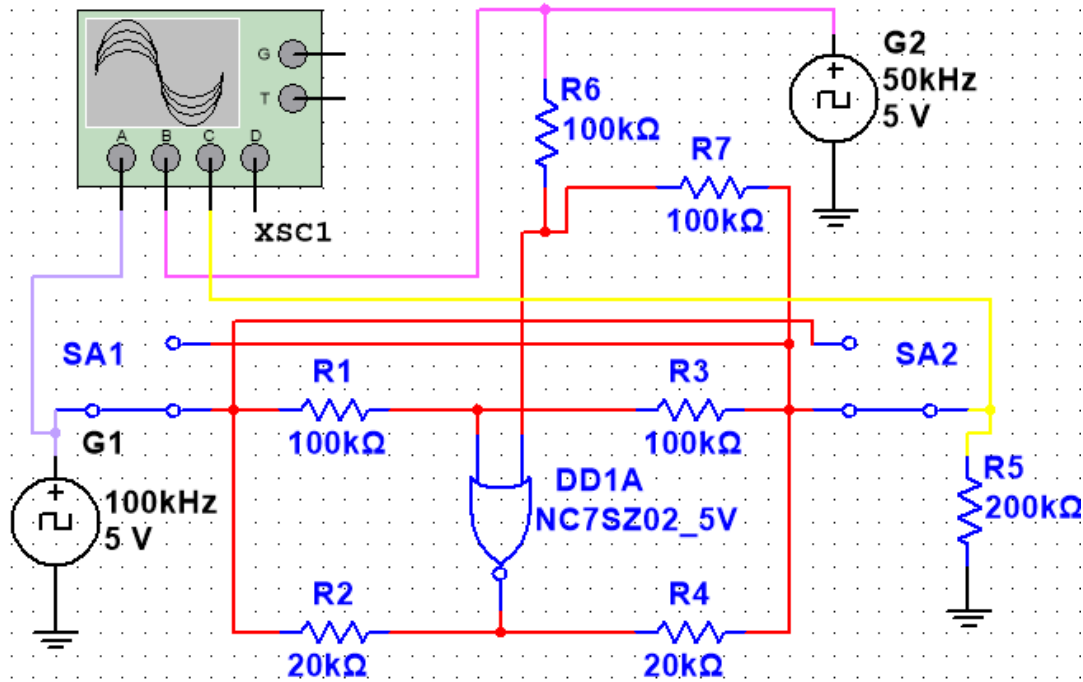**Figure 19**: The scheme of the study of the logical element NOR direct inclusion



**Figure 20:** The Oscillograms of operation of a logical element NOR in the mode of direct inclusion

Figure 21 shows a diagram of the study of the logic element NOR (NC7SZ02) in the mode of direct inclusion, in the case when both inputs are logic signals time variables. The frequency of the first signal is 2 times higher than the frequency of the second signal, which allows us to investigate the properties of this logic element for all possible combinations of logic signals at both inputs. Figure 22 shows the timing diagrams of the logic element NOR in direct connection when connected to both inputs of the sources of logic signals with different frequencies. Such a logic element is characterized by voltage emissions of 0.26V at times when both inputs have a logic unit and small short-term (duration 6.5ns) voltage emissions when the input signals change to opposite values. Thus, by analyzing the output signal for delays and voltage emissions, you can great reliability obtain information about the input logic signals at a given time.



**Figure 21:** The scheme of the study of the logic element NOR direct connection when connecting two signal sources
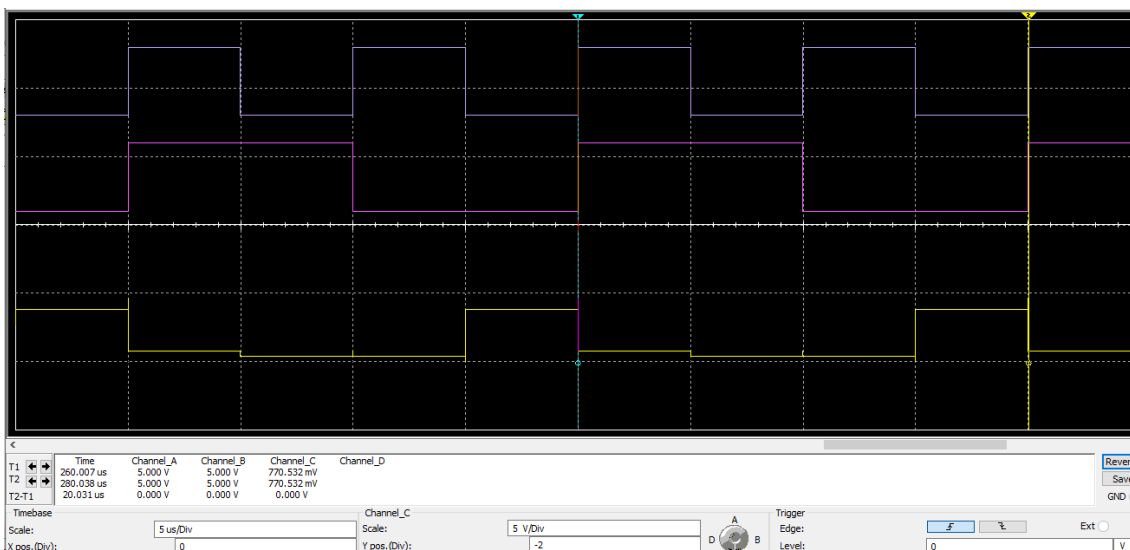


**Figure 22:** Oscillograms of the logic element NOR direct connection when connecting two signal sources with different frequencies

To study the circuit of the logic element NOR (NC7SZ02) (Figure 21) in the reverse connection you need to turn the switches SA1, SA2 in the opposite state. Figure 23 shows the timing diagrams of the logic element OR in reverse when connected to both inputs of the sources of logic signals with different frequencies. Voltage voltages of 0.26V with a delay of 6.5ns characterize such a logic element at times when there is a logic unit at both inputs and small short-term voltage emissions when the input signals change to opposite values.
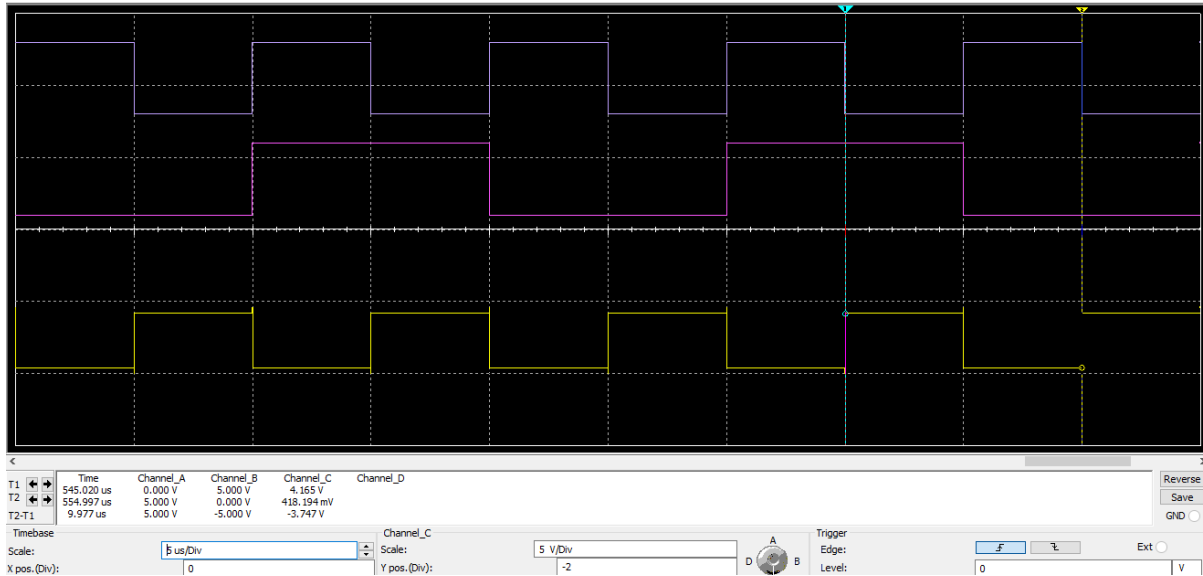


**Figure 23:** Oscillograms of operation of a logic element NOR in reverse inclusion at the connection of two sources of a signal with different frequency

The results of the study of the basic element NOR show that it can work as an inverter, or as a classical element NOR when applying to its input arbitrary variables in time logic signals. However, it is not able to work in normal mode, when one of the inputs will be rigidly installed logical unit. When this is enabled, it, according to the logic of operation, should always output a logical zero, but works as a buffer, but with a significant sag of the output voltage. The advantage of this switching scheme is that when analyzing the output signal, namely the analysis of voltage emissions, you can tell exactly what signals were on each of the inputs of the logic element at a particular time, i.e. this element can store information about the input signals in the output as well as well as the element NAND.

The circuit of the reversible logic element NOR is limited to a maximum frequency of 180 MHz.

The power supply of logic elements operating in reverse mode can be carried out both in the usual way, from DC power supplies (Figure 24, *a*), and one or more external pulse signal generators (Figure 24, *b*), by summing them, for example, adder and subsequent filtration filter R1C1 [20]. Such a load will not affect the shape and amplitude of the signals of the generators. Note that the diode-resistive circuit protection of the inputs and outputs of CMOS chips allows their operation in low-current modes without the use of its power supply when applying signals to the input(s) of the chip.

## 4. Conclusions

Despite the indisputable achievements of the last 10 years in the development of the theory and practical implementation of neural networks, they remain the subject of further intensive research. The neural network proposed by D. Hopfield was compared either with spin-glass – a metastable physical system, or with an associative memory-model of the nervous system of the brain. For a long time, it was ignored, because neural networks were seen as a means of solving applied problems through learning, in which the Hopfield neural network was inferior to the more flexible multilayer networks of direct propagation.
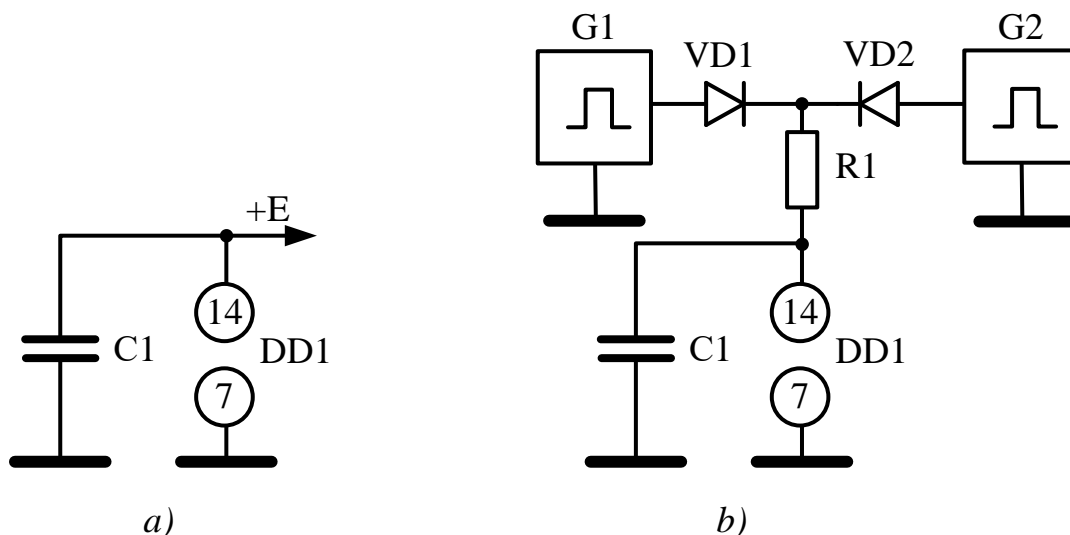
**Figure 24:** Options for connecting the power supply to the chips: *a*) a typical power on; *b*) organization of power supply from generators

Building neural networks of this type require bricks that will consist of the entire structure. Such elements can be even usual logical elements if to use special schemes of inclusion. In the real scheme, the resistances of the n-p junctions of semiconductor transistors, and the switches control signals using multiplexers or other logic switching elements must replace the resistors.

A study of the reversible operation of logic elements has shown that they can work equally in both direct and reverse inclusion. In this case, the two-input elements can output information, in the output logic signal, about the state of the inputs at a given time. To obtain reliable information about the state of the inputs, you need to analyze the output signal for delays and sagging of the level of the output logic levels based on the logic of the logic element.

For such elements there is no difference between input and output, the main thing is to ensure the ratio of resistance between the signal source and the load.

The main task of this work was to show in principle the possibility of using ordinary logic elements in reverse mode. Because of the simulation, it was proved that the logic elements could work in reverse mode, using a special circuit of resistive dividers.

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