Implementation of High-Speed DAC for High Bit Resolution Two-step Flash ADC Applications

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Abstract

This paper reports the current steering DAC design for low power and high-speed aid in maintaining a steady load current and achieving a greater rate of activity. The power drawn can be limited by selecting a low attraction of current for LSB. Keeping these contemplations in view, an 8-bit current steering DAC has been considered. It has been tracked down that this DAC needs a power supply of 1.8 V with a hardness of ±1 mV to bring about a difference in less than 1 µ A (under 0.5 LSB) at the yield of the DAC. Further, the current that will be provided is about 1.78 mA. The DAC and the power supply have been coordinated and the INL, DNL of the DAC are discovered to be inside ±0.4 LSB and ±0.9 LSB separately. The most extreme speed of operation of the DAC is 1GHz with a power utilization of around 9.12 mW using Symica and Ltspice simulation tool.

Keywords

Current-steering DAC, Small chip area, high-speed DAC, and Low power DAC.

1. Introduction

Most of the physical signals are continuous in the time domain is called analog, but digital electronic systems are playing a crucial role in the present communication to process the signal. The process of these analog signals through the communication systems needs to converts the signal from analog to digital (A/D) and after process back to analog by using a digital to analog (D/A) converter. At the end of the signal process, it needs a high-speed D/A converter with high accuracy, linearity, reliability, low power, and so on for high bit resolution two-step ADC design application [1]. Among the different DAC architectures of current steering architecture, charge scaling architecture, and voltage scaling architecture, a binary-weighted current steering architecture was considerable for high-speed application [2]. In this current steering, DAC uses a weighted current source produced by current mirrors to generate the reference current and the MOS transistor switches can control the current. The switches are controlled by the input bits Di showed in figure 1 [3]. Every weighted current source is weighted by 2^0, 2^1, 2^2, 2^3…2^N where N is the number of bits.

2. Design of Current Steering DAC

This design comprises weighted current delivered by current mirrors, changes to control the current, and a viper. The switches are regularly MOS semiconductors. The switches are constrained by the information bits. In the figure, twofold weighted current sources are created by the utilization of current mirrors [4]. This implies that each component is weighted with 2^0, 2^1, 2^2, and 2^3 ... 2^N where N is the number of pieces. The yield current is given by

$I_{out} = b_0 I_u + b_1 2^{-1} I_u + \ldots + b_N 2^{-2} I_u$

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In Figure 1, an N-bit current-directing DAC has appeared. The current sources are current mirrors executed utilizing MOSFETs [7].

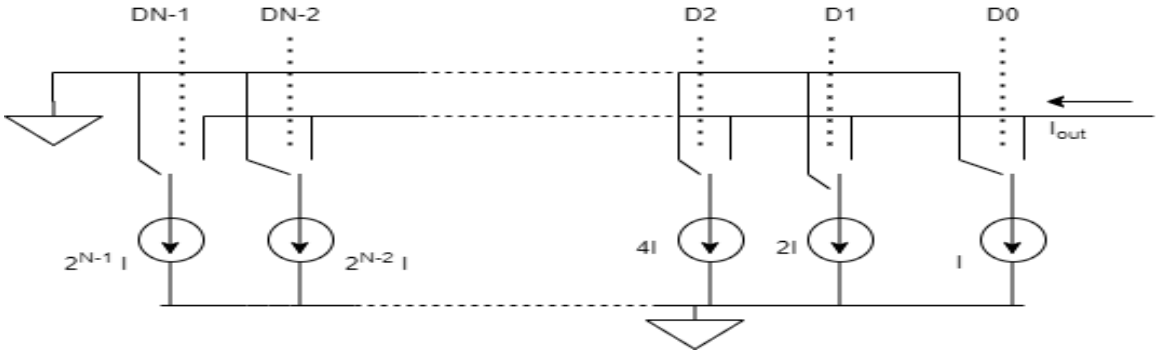

Figure 1: A Current Steering DAC utilizing Binary-weighted Current Sources.

3. Literature Review

[PiyushMathurkar, 2015] The author presented here an improved dynamic performance current steering DAC with a high conversion rate, constant output impedance, and high linearity. [Leila Sharifi,2016] the authors presented a high-speed current steering 8 bit DAC, with high sampling speed and low chip area and simple layout method while incorporating modules using current mode binary to thermometer decoder.

Table 1

Comparison with other DACs.

References	[8]	[6]	[7]	[8]	[9]	Proposed work
Resolution bits	8	8	8	8	8	8
Sampling frequency(Hz)	100M	100M	500M	12G	100M	1G
Supply(V)	3.3	3.3	1.8	1	3.3	1.8
SFDR in dB	53.4	62.13	35.42	51	54	118.24
Power(mW)	27.5	54.5	..	190	45	24.42
Technology(um)	0.35	0.35	018	0.09	0.35	0.13
DNL in LSB	0.31	0.12	0.137	0.28	0.15	0.9
INL in LSB	0.26	0.32	0.331	0.31	0.15	0.4

4. Result Evolution

The parallel-connected three NMOS transistors M2, M3, and M4 shown in figure 2 act as switches S0, S1, and S2 to control the currents, and these switches are controlled by the previous binary to thermometer decoder [8]. The current I0 is reflected from I1 of the current mirror transistors M0 and M1. The transistors M2, M3, and M4 are switched ON when the practical path is disconnected from transistor M1 to the ground. For the switches "S2S1S0" is "001" it means switch M2 is conducting and appeared between M1 and ground, for two-bit, i.e. four combinations thermometric combinations (S2S1S0) are (111), (011), (001), and (000) accordingly the current I1 drawn by M2, M3, and M4 transistors.

The relations of current mirror current I1 and output current I0 are as follows.

Lets K =$\frac{W}{L}$ and the current I0 is

I0 = I1 $\frac{(K)M0}{(K)M1}$ = [(S1 S0) + (S1) + (S1+S0)] Iu,

Now, where Iu is the unit current of 2bit DAC for (S2S1S0) = (001).
The output current is Ioutput from figure6 is

Ioutput = [(B1B0) + (B1) + (B0)] Iu + [(B3B2) + (B3) + (B2)] 4Iu + [(B5B4) + (B5) + (B4)] 16Iu + [(B7B6) + (B7) + (B6)] 64Iu.

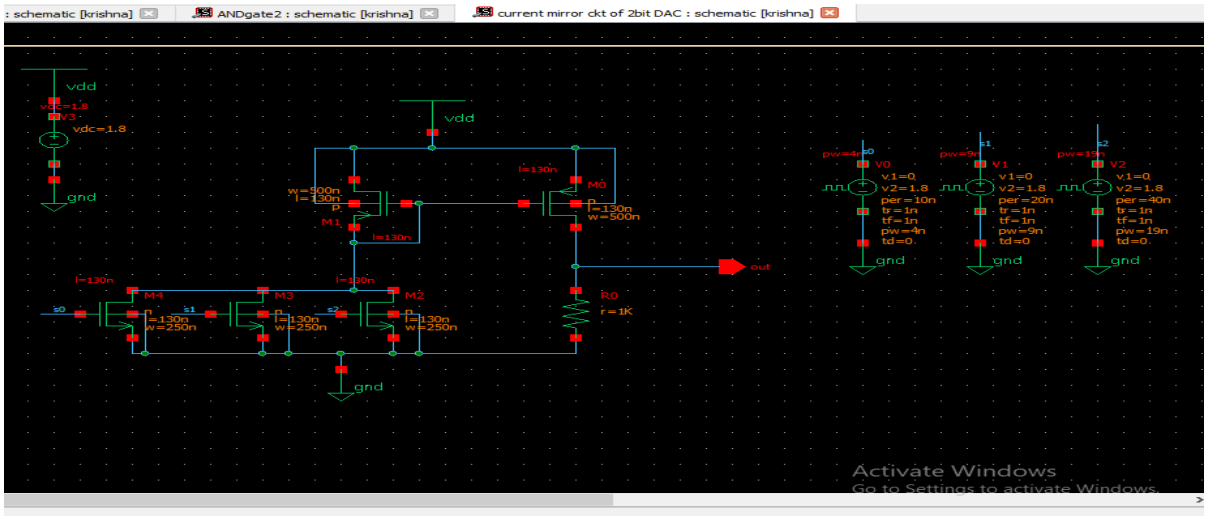

Figure 2: Current mirror circuit of 2-BT Operation output response (CM 2-BT operation)

The current mirror (M0, M1) circuit shown in figure 2 and output response in figure3, current I1 through M1 passes by varying the widths of parallel transistors M2, M3, and M4.

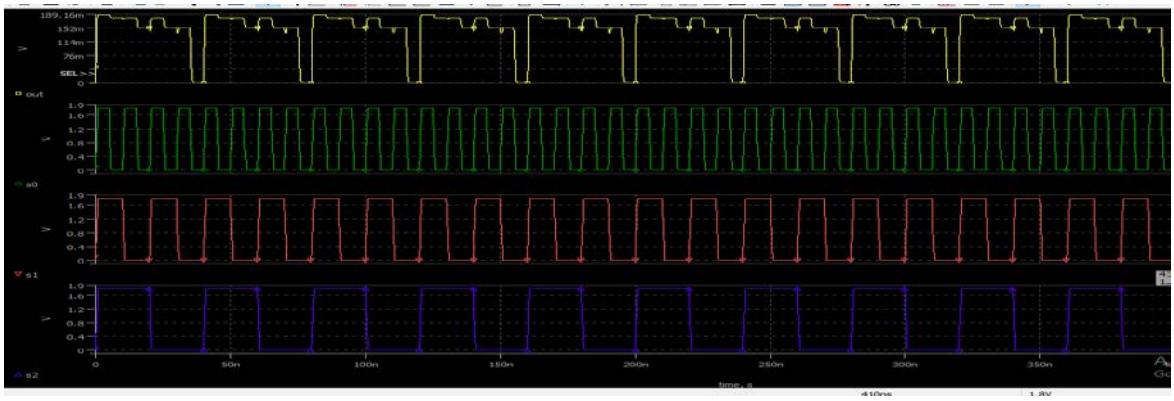

Figure 3: Current mirror circuit of 2-BT Operation output response

5. Binary-to-Thermometer Code Converter

The thermometer code converter shown in figure4 and output response in figure5, for a two-bit binary to thermometer (BT) decoder consists of one AND gate and one OR gate. The outputs of this BT are signals, such as S0, S1, and S2 are the current mirror current control signals. The digital signal mode 8 bit DAC requires just eight AND gates and eight OR gates.

S2= B0B1; S1 = B1; S0 = B0+B1

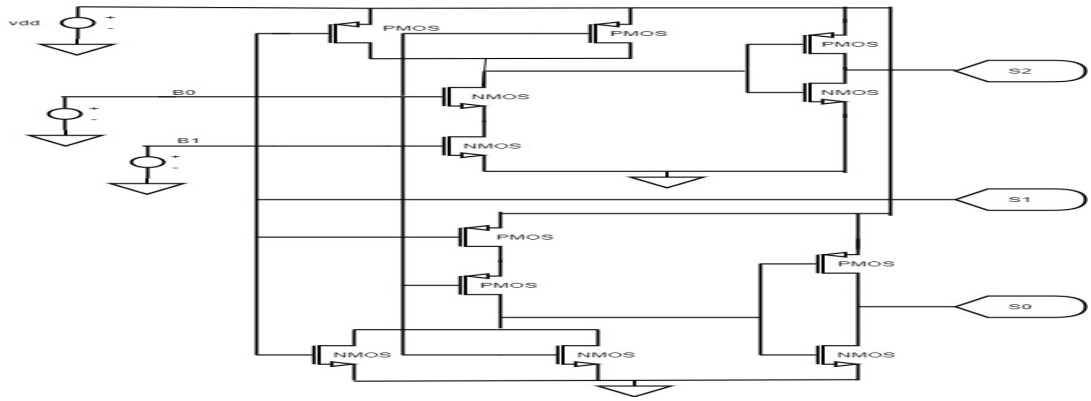

Figure 4: Binary to thermometer coder operation (Mi: BT Code operation)

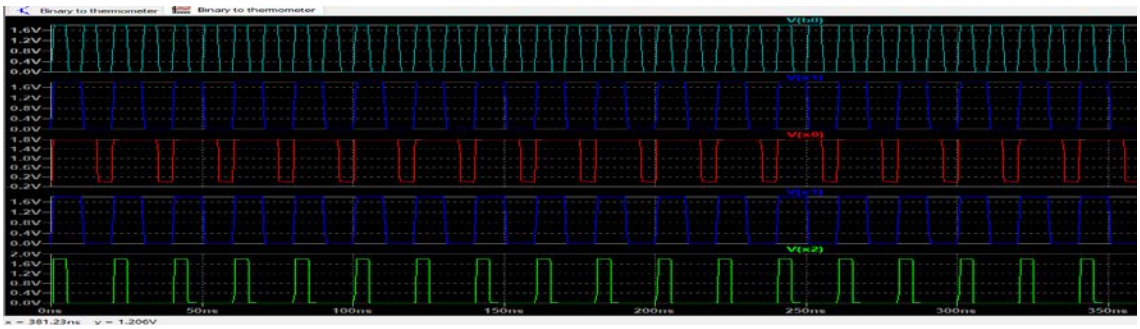

Figure 5: Binary to thermometer coder response

6. 8-Bits Digital to Analog Converter

Figure6 represents a single constructed 8-bit DAC. It had four binary to thermometer decoders modules along with current mirrors, which resulted in a two-bit DAC complete circuit. The DAC required four different current sources, which were explicit Iu, 4Iu, 16Iu, and 64Iu. The suggested improvement may be constructed in a direct presentation using differential mode DAC [10], the spurious-free dynamic range (SFDR) 118.24dB at the frequency of 91.7MHz. Using the modules of figure 2&4 are cascaded as shown in figure6, output response in figure7, and FFT in figure8 for 8-bit DAC design.

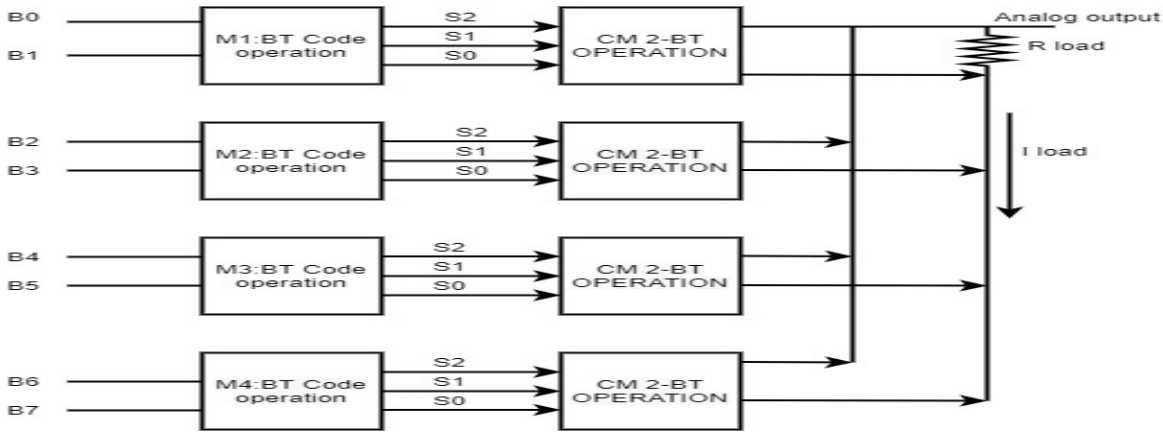

Figure 6: Single-Ended 8-Bit DAC

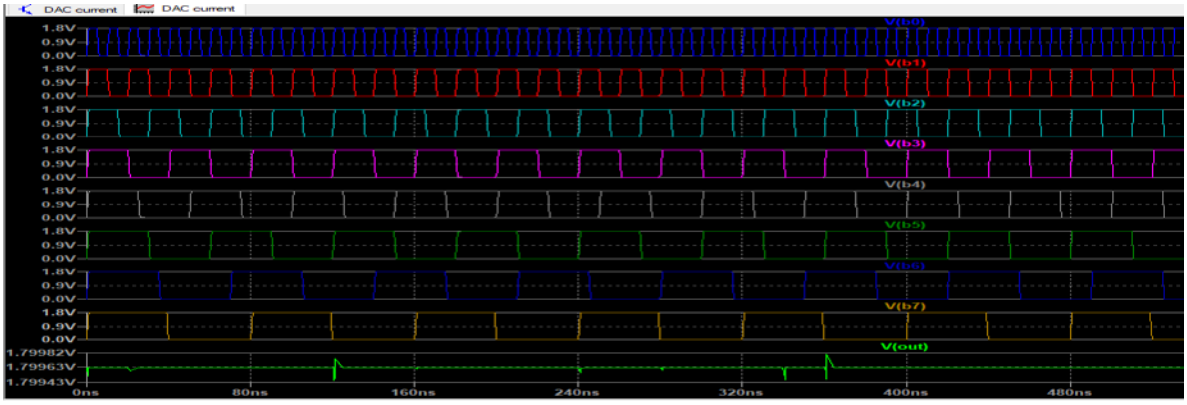

Figure 7: Single-Ended 8-Bit DAC response

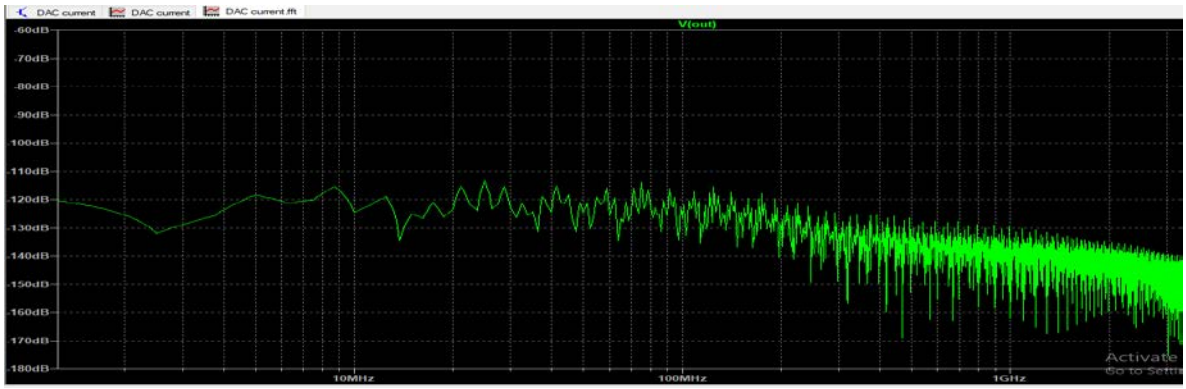

Figure 8: Single-Ended 8-Bit DAC FFT response

7. Conclusion

This paper presents a high-speed low area; low power 8-bit binary-weighted current steering DAC using four BT decoders. In addition, the DNL and INL are acquired equivalent to 0.4 and 0.9LSB, separately. Complete power dissemination of the proposed DAC is just 4.2mW and the dynamic area is to be a small equivalent to 0.23mm2 by utilizing the current mode binary to thermometer decoder. The design simulated in 0.13um CMOS technology with a supply of 1.8v.

8. Acknowledgment

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