Methods for Integration of III-V Compound and Silicon Multijunction Solar Cell

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Abstract

Developing high-performance & economical solar cells are one of the fundamental aims to achieve an economical levelised price of energy. On comparison, it can be easily visualized that silicon based solar cells have just about to reach on the verge of efficiency threshold i.e nearly 25%. On the other side, III-V solar cells are gradually exhibiting performance advancement with an increment of almost 1% per year, with current recorded PCE of nearly 45%. Assimilation of these III-V solar cells on comparatively economical Silicon layer has stimulated massive curiosity towards forthcoming energy plans by coalescing the advantages of III-V constituents with inexpensive & largely available Silicon. This paper will elaborate recent evolvement of III-V cell deposition over Silicon layer. Further, fundamental design principles & the technical contentions *w.r.t* coalition of III-V solar cells on Silicon layer are elaborated. Various methods for coalescing III-V solar cells over Si layer through heteroepitaxial coalition & by mechanical stacking technique are discussed. With reduction in cost of silicon solar cells, complemented with huge space existing for enhancing the III-V solar cell PCE, the forthcoming visions for efficacious coalition of III-V solar cell over Silicon layer seems highly favorable to begin an epoch of forthcoming generation of high PCE & economical solar cells.

Keywords

Multijunction, High Efficiency, III-V-on-Si solar cells, hetero-epitaxial integration, mechanical stacking.

1. Introduction

Today, III-V multijunction solar cells are used as effective technology in space power applications [1]. Although, these cells have exhibited the highest energy conversion efficiency among all the available solar cells, yet their expensiveness has been the principal barrier in their extensive use in terrestrial applications. As already discussed, single junction/monojunction (1J) Silicon solar cells have exhibited PCE of 25.6% which consists of 0.6% improvement in efficiency during the last 15 years [2]. Systematic design of Single Cell is illustrated in Fig.1. However, III-V solar cells have gradually exhibited improvement at the rate of 1% efficiency increase per year, with record 44.7 % efficiency at 297 suns by a 4J III-V solar cell [3]. Further, the supremacy of silicon cells in market with reducing cost in current scenario has challenged the III-V solar cells to create a robust commercialization effect. Expensiveness of starting substrate i.e. GaAs and Ge results in expensive III-V solar cells. Effective combination of III-V solar cells over Silicon layer offers a huge potential for reducing the future levelized energy price by combining advantages of group III-V constituents with inexpensive & largely available Silicon substrate. Silicon not only possess significantly low price corresponding to the larger area & cheaper Silicon substrate, but also have the properties like better mechanical strength & higher thermal conductivity compared to Ge & GaAs substrates. III-V solar cell coalition over Silicon layer may possibly utilize Silicon layer as an active lowermost sub cell.

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Possessing a bandgap of 1.12 eV, Silicon layer may be considered as a better lowermost cell contender compared to Germanium layer possessing 0.67 eV bandgap, for coalition with 2J InGaP/GaAs solar cell. The subsequent trio-junction InGaP/GaAs/Si formed are swiftest path for III-V-on-Si solar cells [4] carrying hypothetical efficiency more than 40% in AM1.5g & AM1.5d [5]. Current research has unveiled that shifting from a four inch Ge substrate to an eight-inch Si substrate will result in 60% decline in price for multijunction solar cells [6].

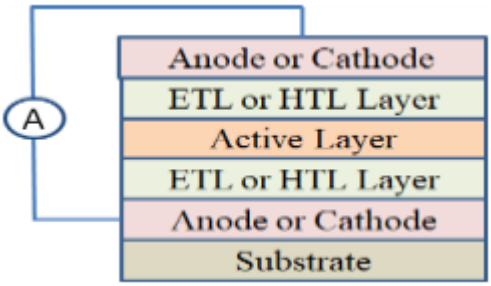

Figure 1: Schematic design of Single solar cell

The exploration w.r.t coalescing III-V over Silicon layer for PV use was started during 80s. Nevertheless, the intricacy linked with the constancy, material growth & manufacturability result in declination in further exploration of III-V over Silicon solar cells during late 90s. During the past 5-6 years, III-V over Silicon solar cell, exploration for the same has again conferred attention *w.r.t* work on recent buffer technique & mechanical stacking methods. Including reduced price of Silicon, in association with remarkable scope existing for enhancing efficiency of III-V solar cells, forthcoming prospects for efficacious coalition of III-V over Silicon layer seems highly encouraging. This paper elaborates technical challenges and design criteria linked with coalescing III-V solar cells over Silicon layer. Further, various processes for coalescing III-V solar cells over Silicon layer through heteroepitaxial coalition & through mechanical mounding is elaborated. Finally, opportunities and future prospects towards further advancement of the efficiency of III-V solar cell over Silicon layer are presented.

2. Design criteria

Fundamental methodologies for coalescing III-V-on-Si substrate solar cellsare: heteroepitaxial growth (or monolithic) & mechanical stacking (wafer bonding). The subsequent segments analysis the fundamental design phenomenon & technical hitches linked to the abovementioned coalition techniques.

2.1. Heteroepitaxial integration technique

Heteroepitaxial integration approach is alleged as very encouraging way to assimilate III-V solar cells over Silicon layer utilizing mono substrate & single epitaxial method [9]. Lattice- matched InGaP/GaAs solar cells are the basic ingredient in 3J and 4J III-V solar cells. Figure 2 illustrated the schematic design of the trio- junctionGaInP/GaAs/Si solar cell [5]. Therefore, it can be easily assumed that coalition of GaAs over Silicon layer was the preliminary & normal option for establishing a strong stage for the forthcoming multijunction solar cell development [10]. Current methodologies that include metamorphic graded buffers *viz*GaAsP and SiGe are receiving a huge attention for III-V over Silicon solar cells [11]. Other heteroepitaxial coalition techniques, which are yet to be extensively explored are as follows-(i) lattice-matched dilute nitride solar cells over Silicon layer [12], (ii) lattice-mismatched InGaN solar cells over Silicon layer [13, 14].

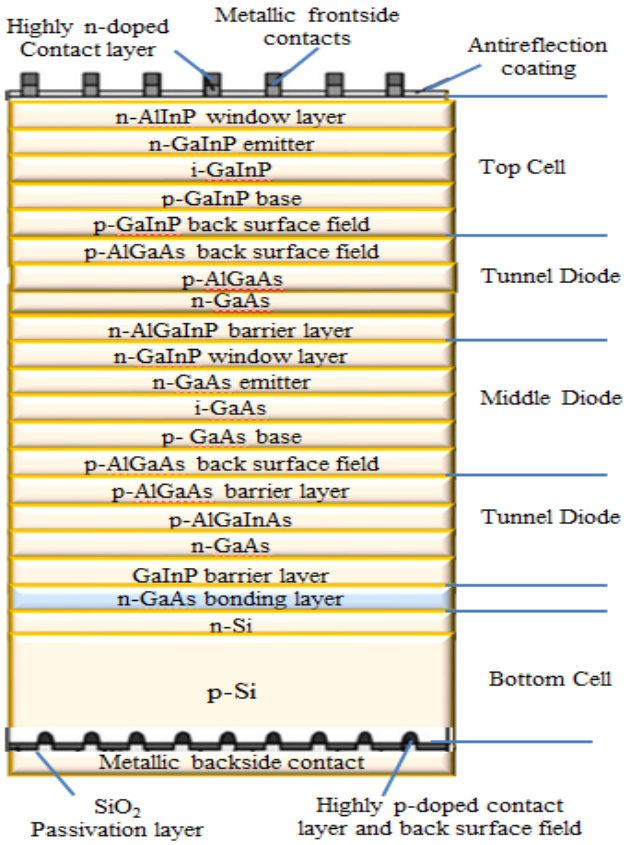

Figure 2: Schematic design of the trio junction GaInP/GaAs/Si solar cell

Most discerning obstacles linked to heteroepitaxial coalition of III-V materials over Silicon layer are as follows:

2.1.1. Growth of lattice-mismatched III-V-on-Si substrate materials

Lattice-mismatch of 4% among Si & GaAs &materials force the direct lattice growth of GaAs over Silicon layer awfully difficult, causing in creation of threading & misfit dislocations which have a pernicious effect on the carrier lifespan & subsequently on PCE. The popular methods employed for GaAs lattice growth over Silicon layer to decrease the defect & dislocation density incorporate annealing, [15] the low growth rate technique and low temperature throughout the preliminary GaAs nucleation over Silicon layer [13]. Developing denser GaAs buffers results in dislocation declination [13] however this results in cost inflation & increase the time of the epitaxial method. Figure 3 illustrated the mechanisms of dislocation motion in III-V surface heteroepitaxially grown on Silicon layer [16]. Furthermore, thin strained films and superlattices added to the dense GaAs buffer results in the eradication of TDs & reduce dislocation distribution in active films. These methods result in maximum PCE *w.r.t* heteroepitaxial monojunction GaAs over Silicon solar cells [16]. Current methods comprise of the development of metamorphic graded buffers to link the lattice constant among Silicon & GaAs/ GaAsP layers [11]. In this regard use of graded SiGe buffers leads to reduction in dislocation, however, these buffers are dense. In addition, these have lower bandgap which prevents the use of silicon substrate to be used as bottommost cell. GaAsP buffers have larger bandgap which may evade the condition of using Silicon substrate as an active sub cell.

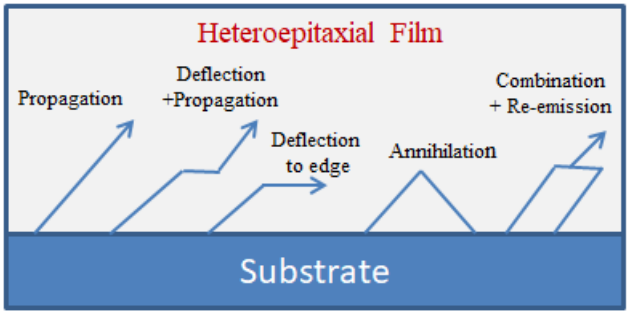

Figure 3: Mechanisms of dislocation motion in III-V film heteroepitaxially grown on Si substrate

2.1.2. Heteroepitaxy of polar III-V materialson Ge/Si substrate

Development of multiatomic, heterogenous semiconductors(SC) over monoatomic semiconductors consequences in emergence of structural defects *viz* antiphase domains, produced because of heteroepitaxy of GaAs (polar materials) over Ge/Si (non-polar materials). The plane of Silicon film [001] comprises of monoatomic phase where these atoms of Silicon are organized as dimers aligned perpendicularly through adjacent phases. During the development of GaAs over Silicon layer, the arsenic dimers align themselves perpendicularly across the nearby steps resulting in the generation of Ga-Ga or As-As bonds,which induces the development of antiphase boundaries.

2.1.3. Thermal mismatch between III-V materials & Silicon substrate

Thermal expansion coefficient difference (2.6×10^{-6} °C^{-1} for Siand 5.73×10^{-6} °C^{-1} for GaAs) & lattice-mismatch variation between GaAs and Silicon layer, result in residual strain in the layer of defects & dislocations which leads to imperfect crystalline quality. Thermal mismatch results in formation of microcracks in the GaAs epitaxial layer causing severe problems pertaining to solar cell reliability in addition to restricting the cell area and efficiency. It is important to mention that faster cooling rate stimulates microcrack generation, therefore it is imperative to regulate the rate of cooling to curtail the microcrack generation.

2.1.4. Buffer design-electrical conductivity, optical transparency, thickness, & surface passivation.

Appropriate buffer assortment is very important for successful performance of III-V over Silicon solar cells. Transpicuous & thin buffer layers are required to exploit initial Silicon layer as active cell. Further, the conductivity of the buffer is essential for concentrated PV cell to reduce resistance. Metamorphic arranged buffer technique employs a dense buffer layer to link the lattice constant among III-V materials & Silicon layers. Wide bandgap GaAsP type buffer is superior option compared to low bandgapSiGe buffers for appropriate transparency for active bottom silicon cell [11].

2.2. Mechanical stacking/ mounding approach for III-V over Silicon integration

Mechanical stacking *w.r.t* III-V over Silicon coalition may withstand large volume of lattice mismatch & allows the coalition of materials with appropriate arrangement of bandgap that are devoid of lattice- mismatch constrictions. The vital challenges linked with the mechanical mounding technique for assimilating III-V materials over Silicon are as follows:

1. The temperature of bond should be attuned to the group III-V materials &Silicon substrate.

2. The bonding film should be transpicuous& thin to utilize bottom Silicon substrate as active subcell.
3. For functioning of bi-junction solar cell in concentrated light, it is very important to comprehend the conductive bond films to evade series resistance.
4. Bonding edges must possess minimal surface roughness & should devoid of oxides.
5. Feasible removal of III-V layer & reutilization method with higher yield.

3. Design of III-V & Si solar cell

Silicon usually restricts total current once unified in tandem with bi-junction InGaP/GaAs PV cells in trio-junction arrangement [5, 17]. Therefore, the configuration of lower Silicon subcell is very essential for current-synchronizing in tandem cell configuration. Other role of the III-V over Silicon layer is to function as efficacious optical film, permitting adequate light diffusion, surface passivation, sufficient carrier transfers and, minimizing carrier rebound. Generation of Emitter in the Silicon layer is difficult & various techniques are reconnoitered, *viz* in-situ epitaxial phosphorus diffusion [18], in-situ epitaxial growth of Silicon emitter [19] & ex-situ traditional diffusion. The in-situ phosphorus diffusion is found less intensive for ideal junction formation in Silicon [19, 20]. The upper III-V cell captivate the maximum photons of the optimum wavelength & only high energy photons will diffuseto nethermost Silicon cell, therefore providing lesser impact on J_{sc} of silicon solar cell. Silicon emitters of smaller dimensions are desired to make best use of both V_{oc}&J_{sc} keeping boundary recombination velocity small. Nevertheless, there persists a solid deadlock between improving V_{oc}&J_{sc} keeping interface recombination velocity high [21, 22]. The most essential design technique for exploiting Silicon as an active cell with III-V cells, in a multijunction design is to contrive the rear side of the Silicon layerto improve the rear surface rebound and attain good surface passivation since Silicon subcell usually restricts the current in III-V/Si tandem cell configurations [5, 17].

4. Conclusion

In short, III-V over Silicon multijunction PV cells are recuperating attention because of their ability to look after the forthcoming levelised price of energy and to amalgamate the improved PCE benefits pertaining to III-V compounds with inexpensiveness & adequacy of Silicon. Various methods for coalescing III-V on Silicon substrate are summarized. Essential design configuration, various challenges & different methods are studied to minimize the dislocation density by using thin & transpicuous buffers to comprehend Silicon as active bottom PV cell. Effective use of the nethermost Silicon layer as active cell needs rear side Silicon layer engineering to elevate current density of Silicon cell. Circumspect thought of design challenges will be essential *w.r.t* the realization of forthcoming improved efficiency & cheaper III-V over Silicon layer multijunction solar cells. Various heteroepitaxial & mechanically stacked integration techniques have paved the way to numerous opportunities for new III-V on Silicon layer multijunction PV cell. Current researches in the heteroepitaxial and the mechanically stacked integration technique have made it possible to think about the efficiency more than exceeding 40% under concentrated sunlight, signifying an encouraging future for III-V over Silicon PV cell technologies.

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