Impact of Temperature on the Performance of Tunnel Field Effect Transistor

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Abstract

The study analyses the impact of temperature on the performance of TFETs. In this paper, we propose two InGaAs TFETs and compare their figure of merits with silicon based TFET. Various figure of merits such as subthreshold swing, threshold voltage, ION/IOFF and DIBL are analyzed for temperature range from -25°C to 100°C. In this study, the simulation tool used is silvaco. The comparison of single metal and dual metal InGaAs TFET with Silicon TFET has been reported through this work. The results show that dual metal InGaAs TFET is better than single metal InGaAs and Silicon TFET.

Keywords

InGaAs TFET, subthreshold swing, threshold voltage.

1. Introduction

In nanotechnology, Tunnel Field Effect Transistors (TFET) serve as a better alternative to Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) because TFETs have a low subthreshold swing (less than 60mV/dec), low power consumption, and low off current I_{OFF} [1]. Even though the structure of TFET is similar to MOSFET, but both have different switching mechanisms and due to this switching mechanism TFET is a good candidate for low-power electronic devices.

In n-type TFET, when the gate voltage is applied, electron accumulation takes place in the intrinsic region. The Band to Band Tunneling (BTBT) occurs when sufficient gate voltage is applied. This causes alignment of the conduction band (intrinsic region) with the valence band (P region). To enable current flow in the device, valence electrons tunnel from the P region to the conduction band (intrinsic region). To disable current flow in the device, the gate voltage is reduced which causes misalignment of bands [2].

Studying the impact of temperature on TFET is very important as the various figure of merits like subthreshold swing, threshold voltage, and ON current have a dependency on temperature. Therefore, to operate TFET at its best efficiency, the figure of merits should be at the optimum value in the working temperature range [15-20].

In this paper, we propose two InGaAs TFET devices and compare their figure of merits with silicon TFET. In the proposed InGaAs devices, the one is single metal double gate TFET and the other is dual metal double gate TFET. We individually compare the figure of merits of both these devices with silicon TFET using temperature range 25°C to 100°C by using silvaco simulation tool. The results conclude that dual metal double gate TFET is more efficient than single metal double gate TFET [21-25].

This paper is segregated into five sections. Section II discusses the literature review of the work, section III highlights the methodology used for the work, section IV ponders on the results while Section V gives the conclusion of the paper.

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2. Literature Review

In the past, a lot of work has been done in the nanotechnology regime. Earlier MOSFETs are used extensively in this regime but now in the modern era TFETs have proved to be a better alternative [3]. Aswathy et al. [4] have proposed TFET as an alternative for MOSFETs using gate-controlled BTBT and observed a high Ion/Ioff ratio. Datta et al. [5] have studied the design of TFET and focused on the impact of reliability issues in determining energy efficiency then conclude that Heterojunction Tunnel Field Effect Transistor (HTFET) based logic circuits have better energy efficiency when compared with Si-FinFET technology for operation less than 0.5V [26-32].

Silicon TFETs due to their availability is widely used in the industry both in homojunction and heterojunction devices. Chander et al. [6] have studied the temperature analysis of Ge/Si heterojunction TFET and concluded that at high-temperature heterojunction TFETs are suitable for designing circuits. Bjork et al. [7] have implemented TFET using silicon nanowires grown by vapor-liquid-solid growth method and it has been concluded that with a decrease in gate oxide thickness (100nm to 20 nm) there is an increase in current (by order of magnitude) and a decrease in inverse subthreshold swing from 1200 to 800 mV/dec. Luong et al. [8] have fabricated silicon nanowire complementary gates all around TFET that had suppressed ambipolar behavior and estimated the dynamic yield of the cell.

Over time many more TFETs came into the picture depicting better results in low power application areas. Alian et al. [9] have recorded InGaAs TFET with better sub-threshold swing characteristic over MOSFET and concluded that TFETs are more immune to Positive Bias Temperature Instability (PBTI) degradation when compared with MOSFET. Baek [10] applied the electroplating fin formatting technique to fabricate vertical InGaAs TFET and concluded with excellent combinations of the various figure of merits like subthreshold swing, DIBL, I_{ON}/I_{OFF} ratio when compared to III-V TFETs.

3. Methodology

There are two InGaAs TFET devices simulated using silvaco simulation tool keeping silicon TFET as reference. Both these TFETs vary in metal electrodes, one is single metal and the other is dual metal double gate tunnel field-effect transistor. One simulation takes around 20 minutes to complete with a memory usage of 770 MB.

3.1. Device Structure

In this paper, both InGaAs TFETs have a similar structure size of 90nm. The drain length is 30nm, the channel is 30nm and the source is again 30nm [11]. The silicon TFET has a different dimension set which follows 100nm drain, 30nm channel, and 100nm source which makes the device length to be 230nm [12]. Figure 1 denotes the basic structure of single metal InGaAs TFET and Figure 2 denotes the basic structure of dual metal InGaAs TFET.

3.2. Gate Oxide

For InGaAs, gate oxide taken is HfO_2 which has a high dielectric constant k = 22 [11,12]. The gate oxide length is 30nm and the width is 2nm. For silicon, gate oxide taken is SiO_2 which has a low dielectric constant k = 3.6. The gate oxide length is 230nm and the width is 3nm [13].

3.3. Doping Levels

For InGaAs, the source is heavily $8x10^{19}cm^{-3}$ p-type doped, the drain is $1x10^{18}cm^{-3}$ n-type doped and the channel is kept with intrinsic nature [11]. For silicon, the source is heavily $1x10^{20}cm^{-3}$ p-type doped, the drain is $5x10^{18}cm^{-3}$ n-type doped and the channel is $1x10^{17}cm^{-3}$ n-typed doped [13].

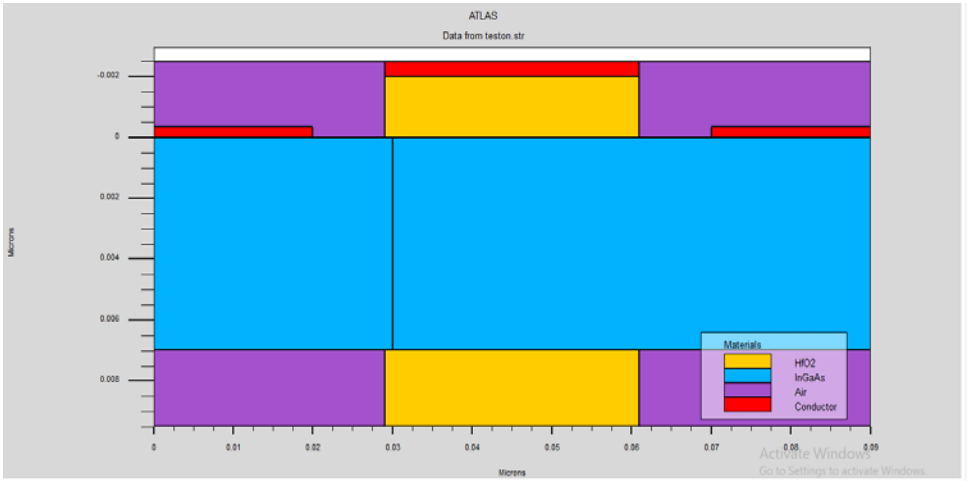

Figure 1 Basic Structure of single metal InGaAs without doping

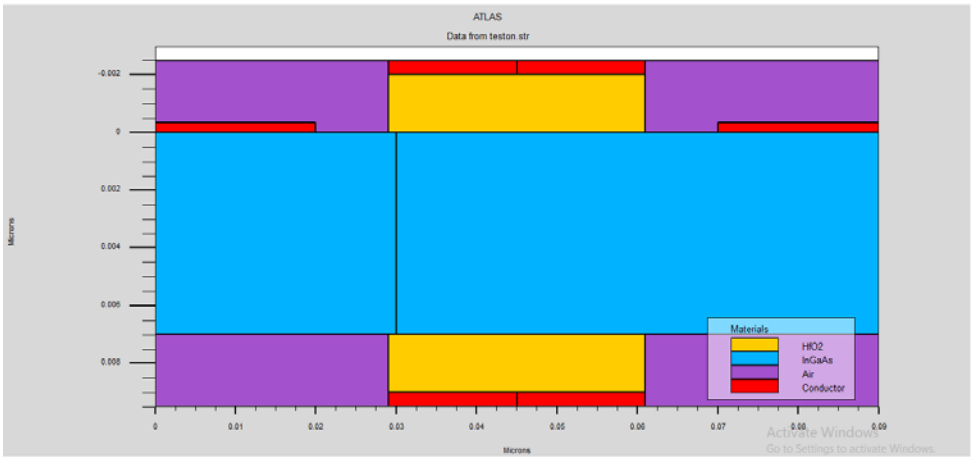

Figure 2 Basic Structure of dual metal InGaAs without doping

3.4. Metal Electrodes

For single metal InGaAs, the metal electrodes used are of copper having a work function range of 4.53-5.10. For dual metal InGaAs, the metal electrode along the source side is Tantalum having a work function range of 4.0-4.80 and along the drain, the side is of copper with a 4.53-5.10 work function range [11]. For silicon, the metal electrodes used are of manganese having a work function of 4.1 [12].

3.5. Figure of Merits

All figures of merits of InGaAs TFET were analyzed in a temperature range of -25°C to 100°C and compared with silicon-basedTFETgraphically.Thevariousfigureofmeritsused for the analysis of InGaAs TFET are subthreshold swing, threshold voltage, ON current (I_{ON}) [1].To increase the output current by one decade, the change applied in gate voltage is regarded as a subthreshold swing. Its physical significance can be understood as the slope of the I_D-V_G graph before threshold voltage. Itsdependenceontemperatureisshownbyequation1.

$$\text{Subthreshold Swing, } ss = ln\frac{KT}{q}\left(1+\frac{C_d}{C_{ox}}\right) \quad (1)$$

In this work, the voltage at the drain terminal V_{DS} is 0.5V and at gate terminal voltage V_{GS} is varied from 0 to 0.5V at a step of 0.01V. With an increase in temperature, threshold voltage decreases and thus depicts a positive temperature coefficient due to changes observed in fermi level and bandgap [14].

For the case of I_{ON}/I_{OFF}, equation 2 describes its relationship with carrier effective mass and tunneling barrier.

$$\text{Drain Current, } I_D = A \cdot V_{GS}^2 \cdot exp\left(\frac{-B}{v_{GS}}\right) \quad (2)$$

If carrier effective mass and tunneling barrier are represented byAandBrespectively,thenequation3and4areas follows

$$A\alpha E_G^{-0.5} \quad (3)$$

$$B\alpha E_G^{1\cdot 5} \quad (4)$$

In semiconductors, the relation between variation of energy gap E_G and temperature (T) is described by equation 5

$$E_G = \frac{E_0 - \alpha T}{(T - \beta)} \quad (5)$$

4. Results

In this paper, all simulations have been carried out in silvaco simulation tool. The simulation values were recorded systematically and then comparison among both InGaAsTFET devices taking Silicon TFET as a reference has been done. The graphs were obtained using originPro software.

4.1. Simulation Results of Single Metal InGaAs TFET

After performing all the simulations, the optimum values of each figure of merit have been reported in Table 1.

Table 1

Performance Parameters of Single Metal TFET

Temperature (°C)	Subthreshold Swing (mV/dec)	Threshold Voltage (V_t)	I_{ON} (µA)	I_{OFF} (nA)	I_{ON}/I_{OFF}	DIBL (mV/V)
-25	40.549	0.153	24.813	1.489	166553.675	278.191
0	42.039	0.150	24.906	2.127	117084.028	283.542
25	43.213	0.147	24.995	2.874	86963.782	289.122
50	44.177	0.144	25.080	3.708	67621.294	295.313
75	44.946	0.141	25.154	4.601	54663.554	301.652
100	45.534	0.139	25.215	5.518	45693.860	307.324

4.1.1 Transfer Characteristics

The graph obtaining transfer characteristics at different temperatures is collected and combined analysis is discussed in Figure3.

It has been observed that the off current increase with rise in temperature. The subthreshold swing obtained is less than 50 mV/dec and is thus indicates better efficiency than silicon TFET. The threshold voltage obtained is less than 0.2V and itdecreaseswith an increaseintemperature [1]. The I_{ON}/I_{OFF} Ratio decreases with increase in temperature. The single metal InGaAs TFET has higher I_{ON}/I_{OFF} ratio than silicon TFET. The Drain Induced Barrier Lowering (DIBL) means increasing drain voltage which results in decrease of threshold voltage of TFET. The DIBL increases with increase intemperature. ThesinglemetalInGaAsTFET has better DIBL than silicon TFET because rise in temperature affects DIBL seriously and thus leads to poor performance of TFET.

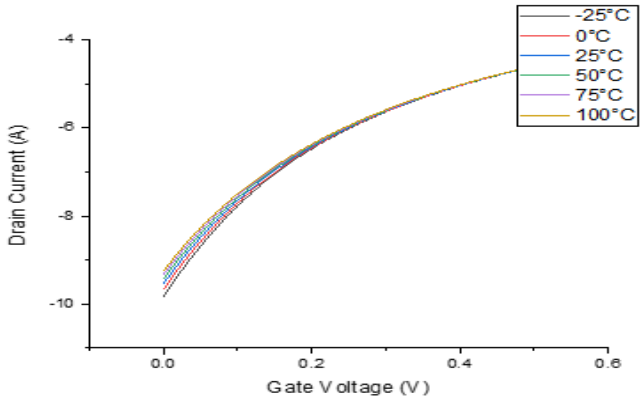

Figure 3 Transfer characteristics of single metal InGaAs

4.1.2 Energy Band Diagram

The band diagrams of single metal InGaAs TFETs are shown in Figure 4. The energy band diagrams are observed both in OFF and ON state. It can be observed that when the device is OFF state the gap between conduction band and valence band of InGaAs is large but as the device is switched ON, this gap reduces and a tunnel is formed through which tunneling of electrons from p+ region to intrinsic region occurs causing BTBT.

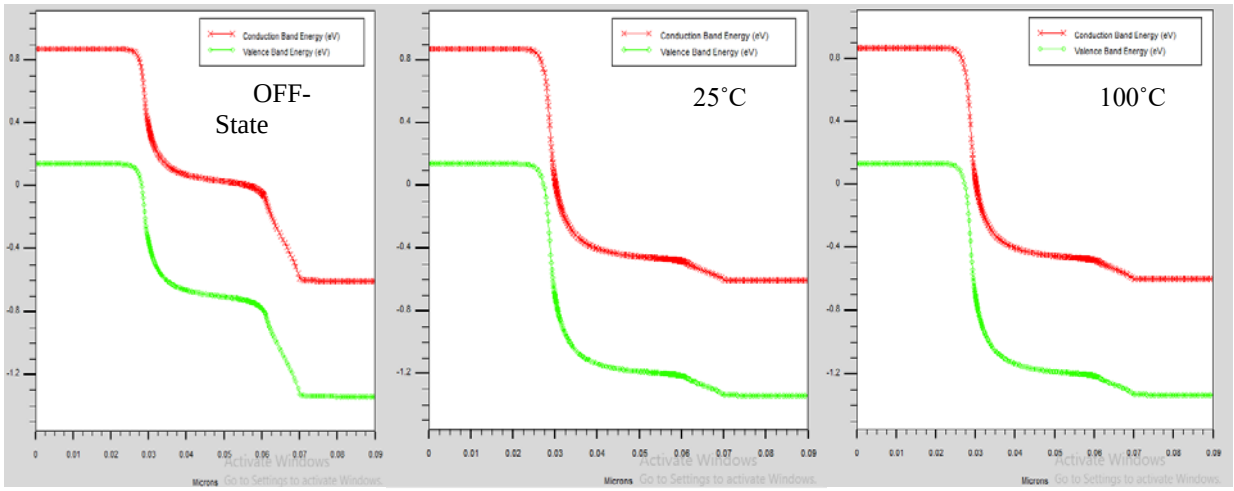

Figure 4 Energy band diagram of single metal at 25˚ and 100˚ C in ON as well as OFF state

4.2 Simulation results of dual metal InGaAs TFET

All the simulations were performed and the best results of each figure of merit were recorded in Table 2.

Table 2
Performance Parameters of Dual Metal TFET

Temperature (°C)	Subthreshold Swing (mV/dec)	Threshold Voltage (V_t)	I_{ON} (µA)	I_{OFF} (nA)	I_{ON}/I_{OFF}	DIBL (mV/V)
-25	36.264	0.144	72.895	0.069	1047442.308	257.744
0	37.153	0.141	72.867	0.098	739532.112	263.112
25	37.814	0.137	72.816	0.131	551725.261	268.774
50	38.315	0.134	72.732	0.168	431304.667	275.414
75	38.659	0.131	72.607	0.206	350947.600	282.281
100	38.927	0.128	72.436	0.245	295469.452	288.634

4.2.1Transfer Characteristics

The graph obtaining transfer characteristics at different temperatures is collected and combined analysis is discussed in Figure5.

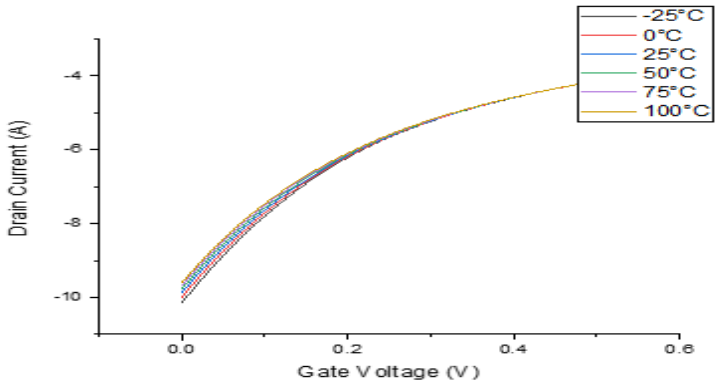

Figure 5 Transfer characteristics of dual metal InGaAs

4.2.2 Energy Band Diagram

Figure 6 has shown the energy band diagrams of dual metal InGaAs TFETs. The band diagrams are studied both in the OFF state and ON state. The conduction and valence bands of InGaAs have a large gap in the OFF state, but as the device is turned on, this gap narrows and a tunnel is created through which electrons tunnel from the p+ to intrinsic area, causing BTBT.

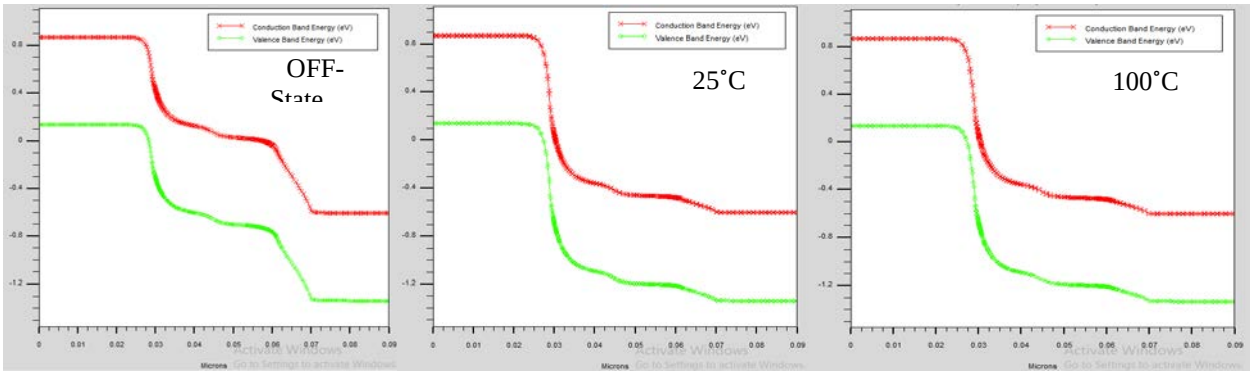

Figure 6 Energy band diagram of dual metal at 25˚ and 100˚ C in ON as well as OFF state

4.2.3 Subthreshold Swing

The subthreshold swing obtained is less than 40mV/dec as shown in Figure 7 and thus indicates better efficiency than both single metal InGaAs TFET and silicon TFET. The subthreshold swing increases with an increase in temperature as shown in Figure 7. At room temperature the SS of SM InGaAs TFET is 43mV/dec and DM InGaAs TFET is 37mV/dec.

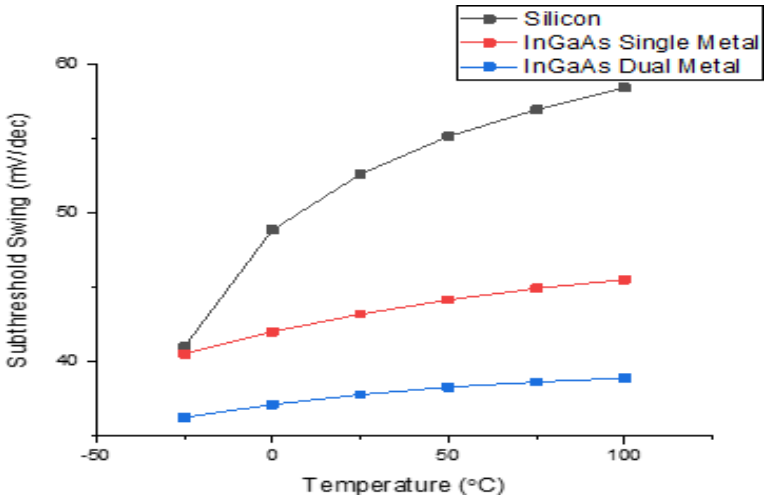

Figure 7 Subthreshold swing Vs temperature

4.2.4 Threshold Voltage

The threshold voltage obtained is less than 0.3V and gives better analysis than both single metal InGaAs TFET and silicon devices. The threshold voltage decreases with an increase in temperature [1] as shown in Figure8.

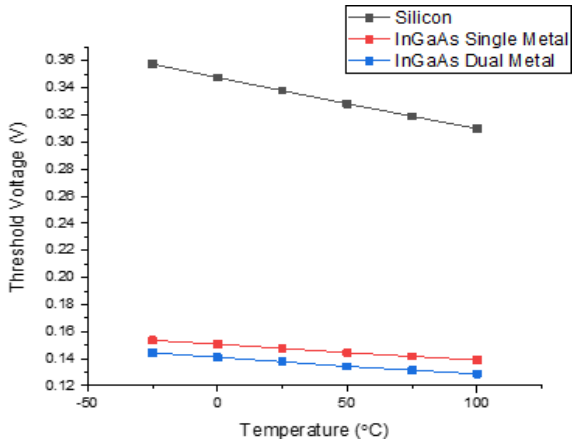

Figure 8 Threshold voltage Vs temperature

4.2.5 I_{ON}/I_{OFF} Ratio

The I_{ON}/I_{OFF}ratio decreases with increase in temperature. The dual metal InGaAs TFET has higher I_{ON}/I_{OFF} ratio than both single metal InGaAs TFET and silicon TFET and graphically it is shown in Figure 9.

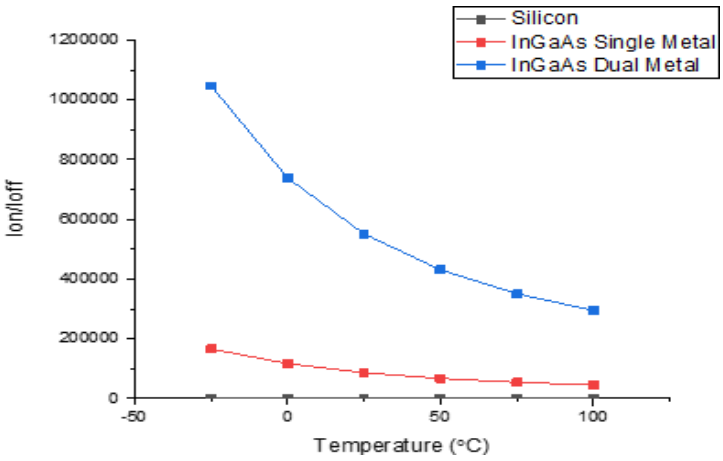

Figure 9 I_{ON}/I_{OFF}ratio Vs temperature.

4.2.6 DIBL

The Drain Induced Barrier Lowering (DIBL) means increasing drain voltage which results in decrease of threshold voltage of TFET. The DIBL increases with increase in temperature [1] as shown in Figure 10. The dual metal InGaAs TFET has better DIBL than both single metal InGaAs TFET and silicon TFET because rise in temperature affects DIBL seriously and thus leads to poor performance of TFET.

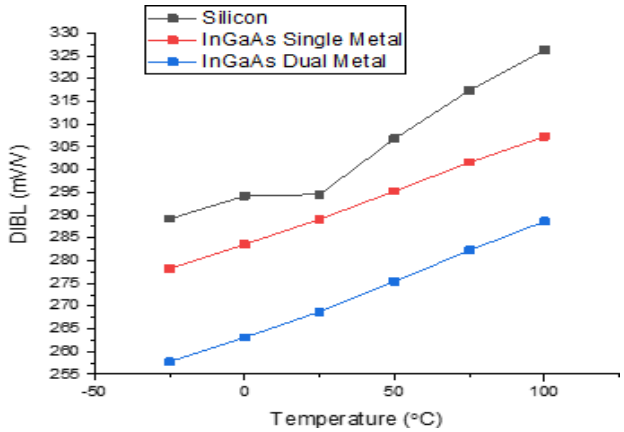

Figure 10 DIBL Vs temperature

5. Conclusion

This paper presents the study of the impact of temperature on TFET. Silvaco simulation tool has been used in this study. The findings of subthreshold swing (SS), the threshold voltage (V_t), I_{ON}/I_{OFF} ratio and DIBL with working temperature indicate that a low-temperature environment is a must for better efficiency of TFET. Furthermore, the dual metal InGaAs TFETs give better results in various figures of merits as compared to single metal InGaAs TFETs and Silicon TFETs when operated under same environment temperature conditions. As a future scope of this study, further investigation can be done by varying the channel length of the TFET devices.

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